TOPOLOGICAL OPTIMIZATION OF INTEGRATED INDUCTORS IN FD-SOI TECHNOLOGY FOR RF AND QUBIT CONTROL APPLICATIONS: USE OF MAGNETIC AND SUPERCONDUCTING MATERIALS AT CRYOGENIC TEMPERATURES

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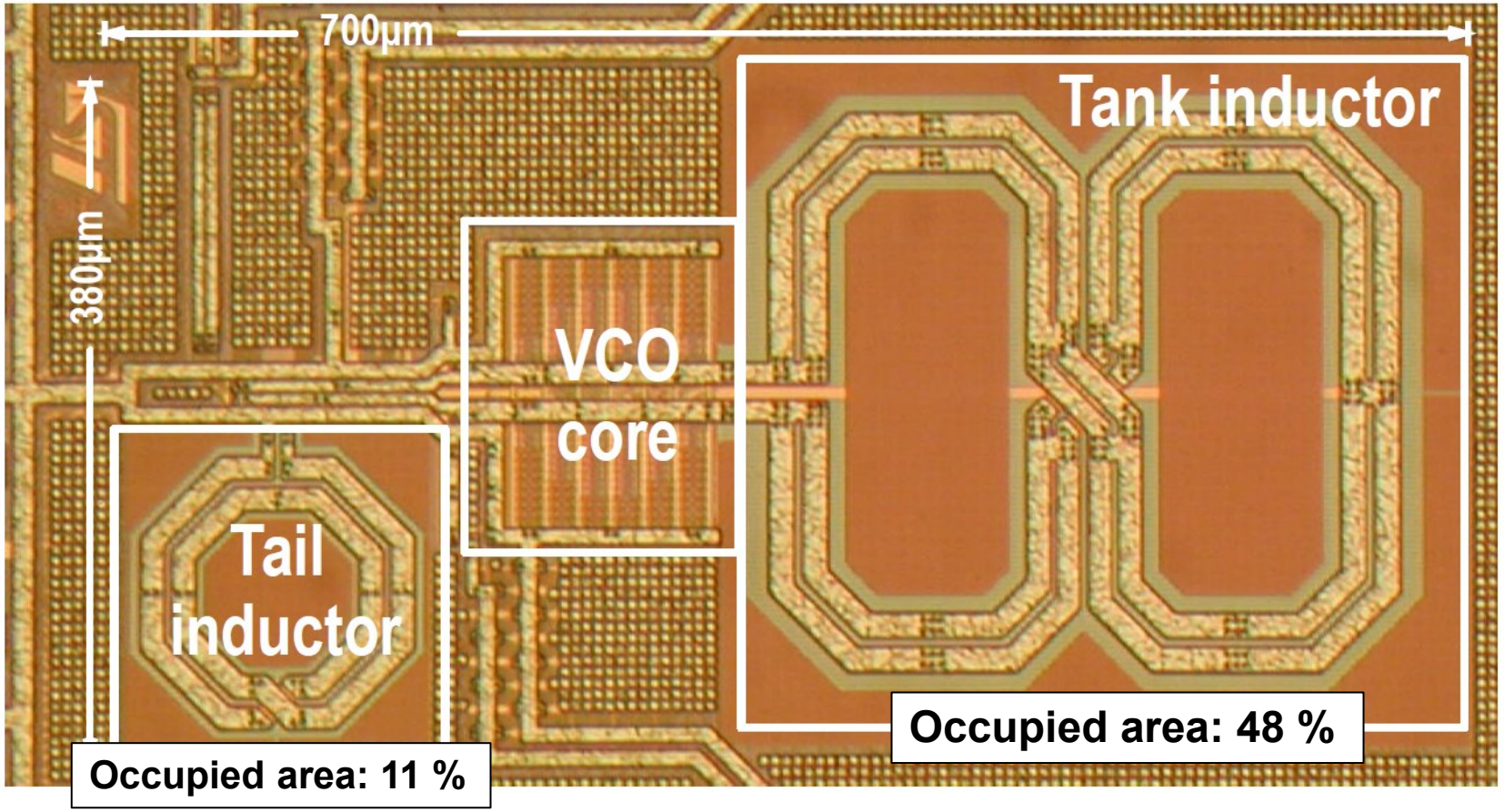
Agenda

- Study context
- EM simulations of identified levers
- NiFe deposition process
- Inductors measurements
- Superconducting thin film silicides
- Innovative gate magnetic structure
- Conclusion and perspectives

Context

Context – Inductors in RF



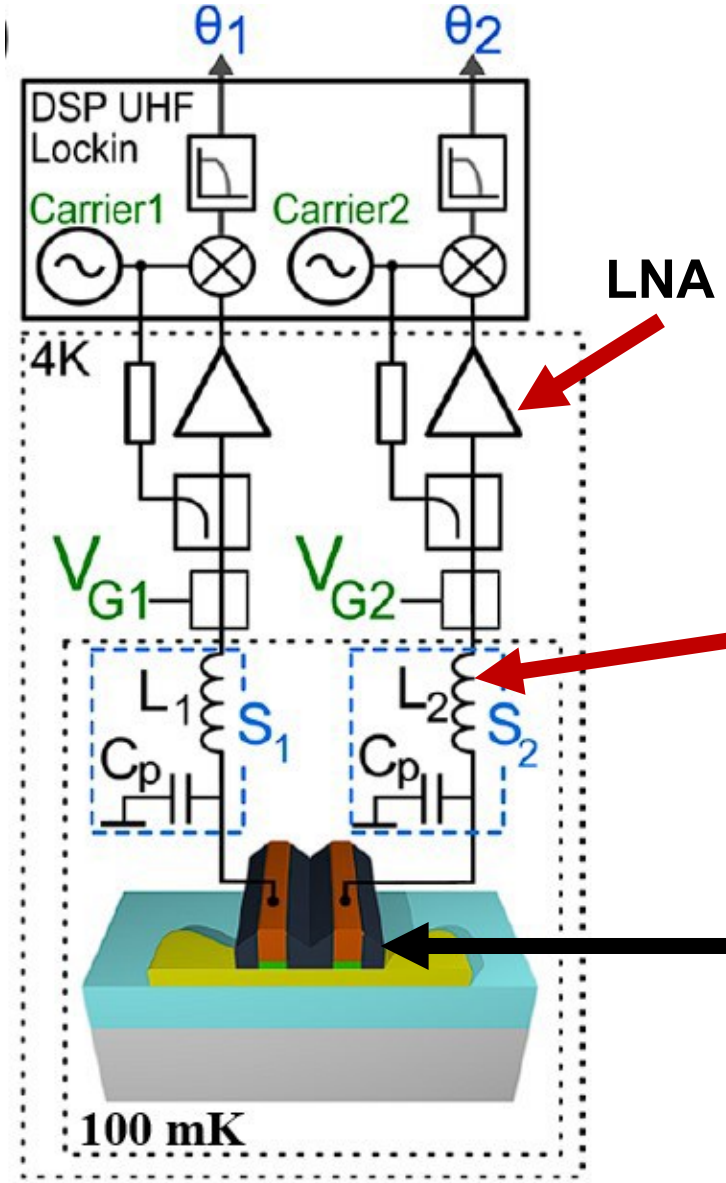
2.8-to-5.8 GHz harmonic VCO in a 28 nm UTBB FD-SOI CMOS process

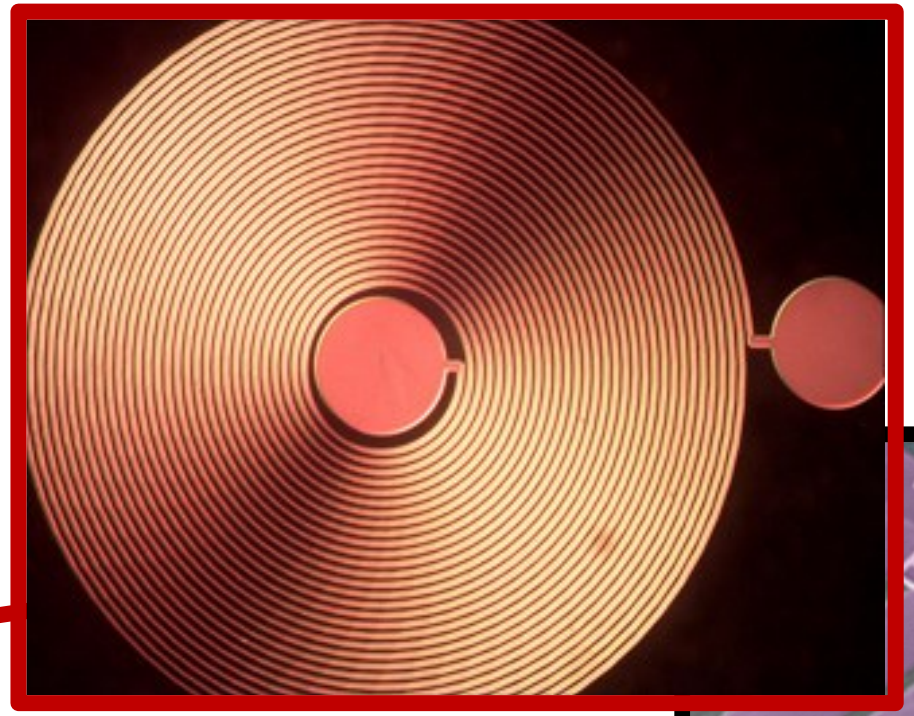
(Operates at room temperature)

Inductor occupy 60 % of area of RF integrated devices

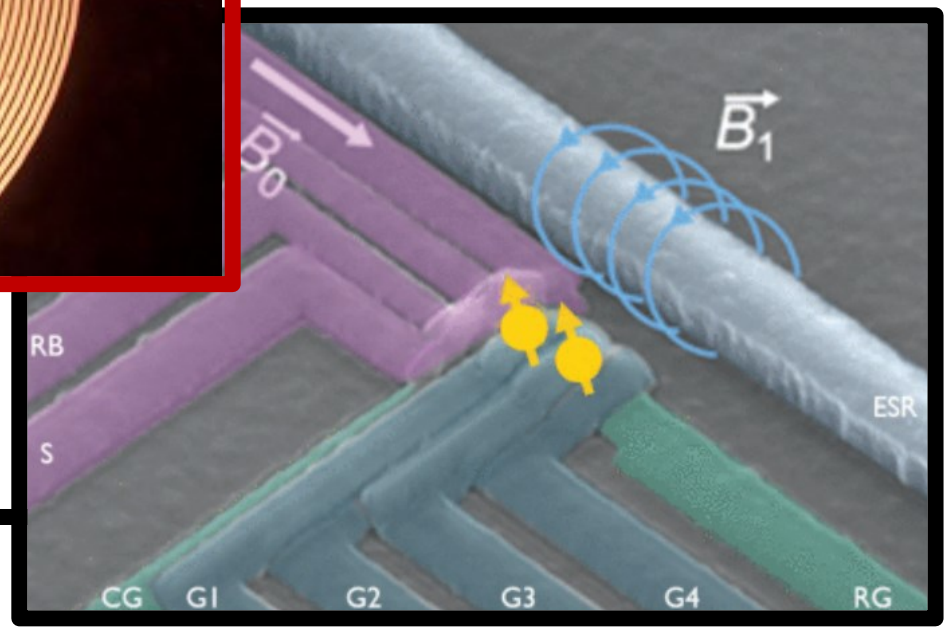
Fanori, L., *IEEE RFIC Synphosim*, [2015]

Context – Place of inductors in quantum





Resonator inductor

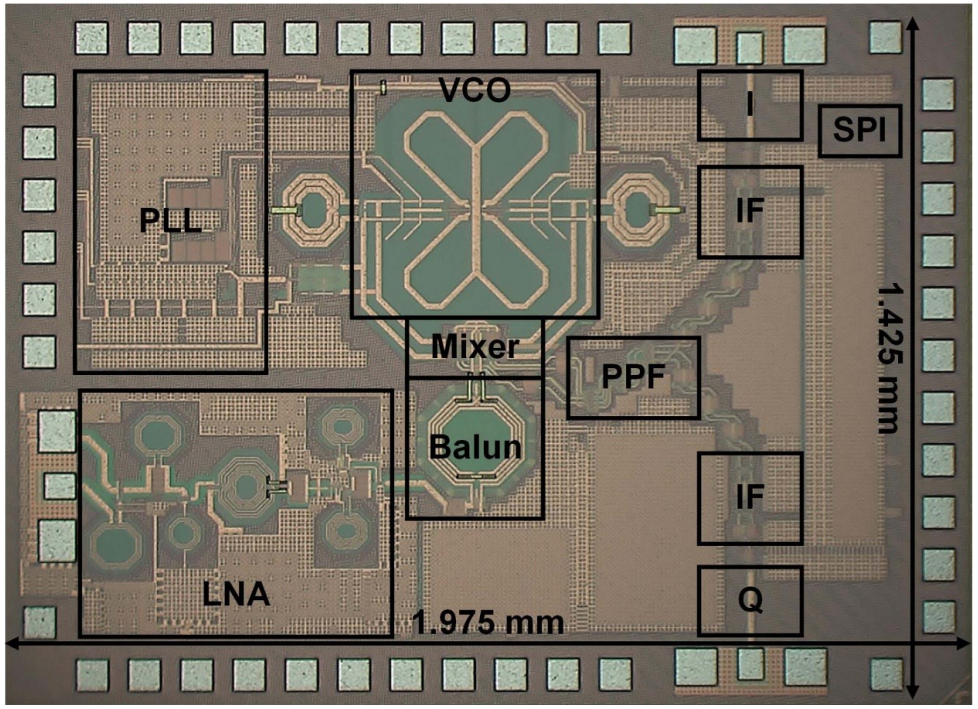


Gys et al., 2022

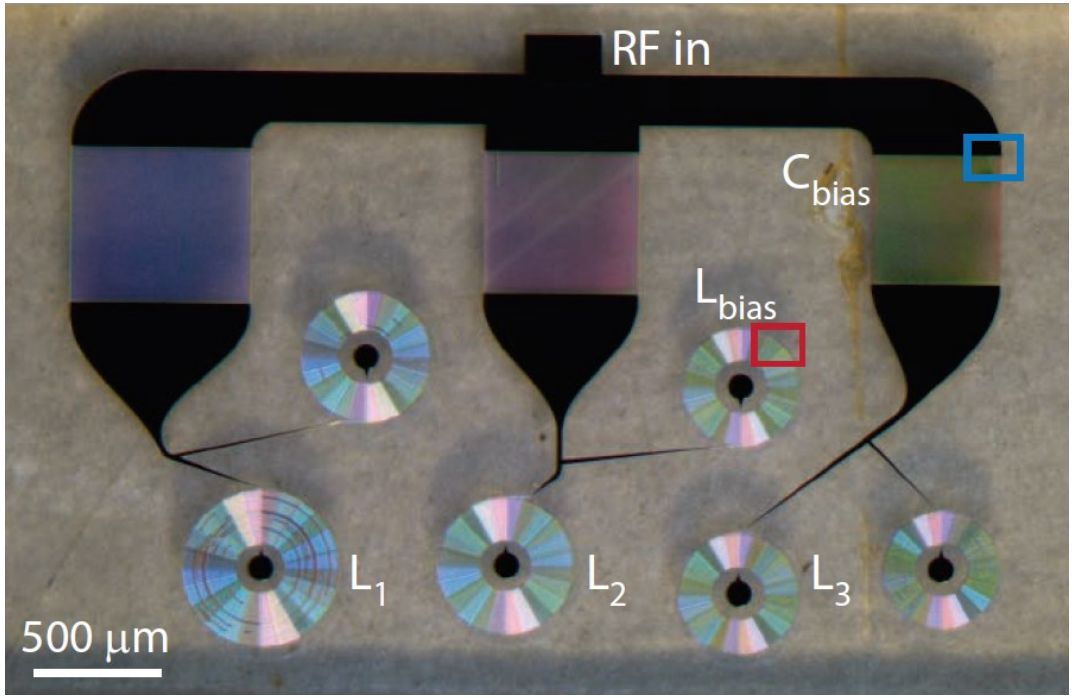
Frequencies of interest:
400 MHz and 7GHz

Inductor are limiting the readout quality

Context – inductor technology for quantum



Cryo-CMOS system for the readout of the state of spin qubits integrated in standard 40-nm CMOS technology

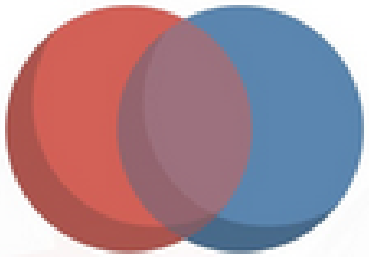


Optical micrograph of the multiplexing Chip using NbN inductors

Different technologies of inductors are used in quantum

J. M. Hornibrook, *Appl. Phys. Lett*. (2014)
Peng Y, *Solid-State Circuits*, [2022]

Context – Quantum computing revolution



Quantum superposition of 2 states

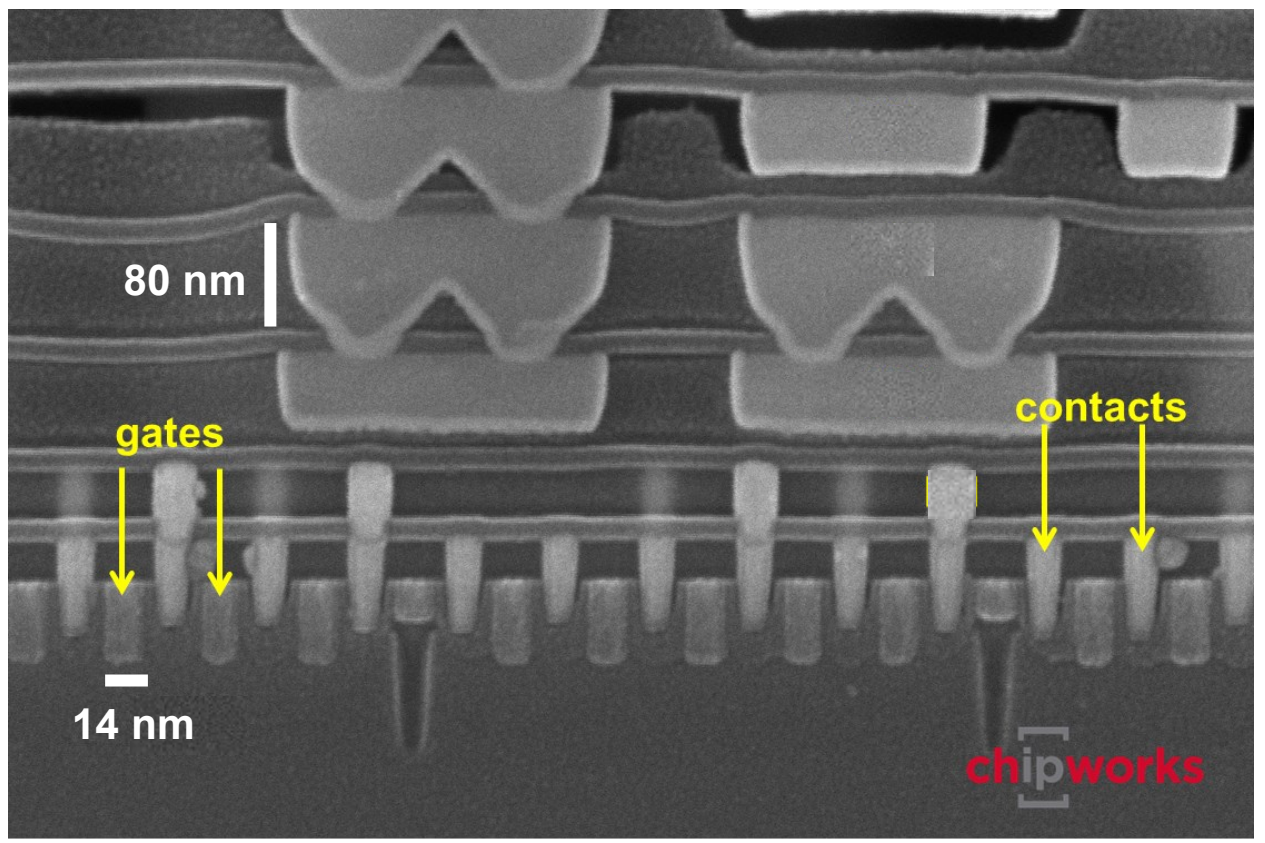
Works at cryogenics temperatures

Field impacted by quantum computing: fundamental physics research, telecommunications, cyber and software security, energy, chemicals, pharmaceuticals…

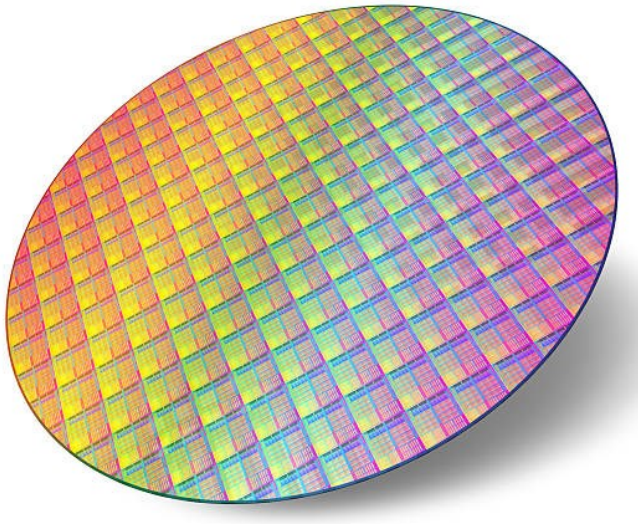
Saltan & Hyrynsalmi, ICSOB Companion [2022]

Quantum computing will bring many benefits in its path

Context - CMOS technology



CPU of the Samsung Galaxy S6 : the Exynos 7420



Wafer

Etienne Sicard, thesis, [2017]

D. James, *chipworksrealchips.blogspot.com*, [2015]

Context – Summary of RF and quantum requirements

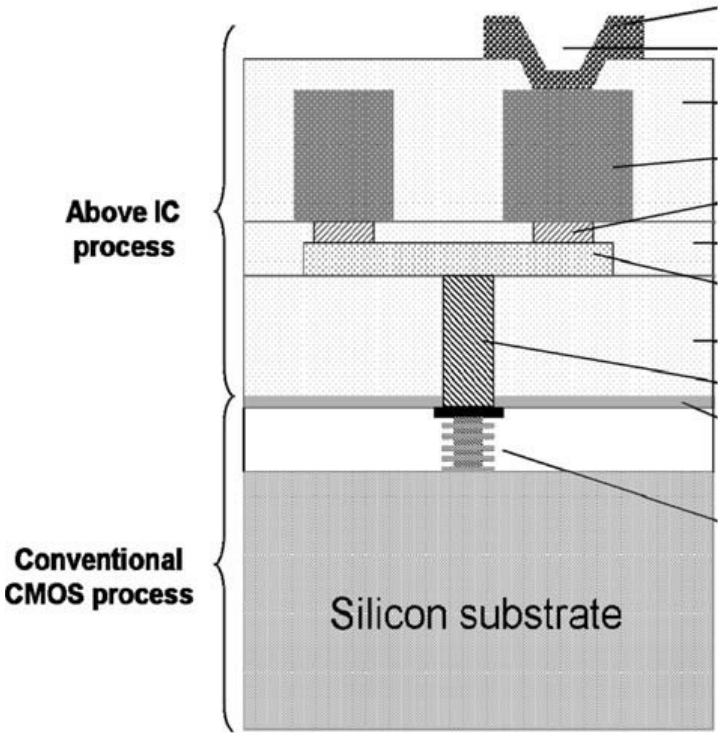
	Inside the LNA	Qubit readout
Inductance	**Few nH**	**80–400 nH**
Q-factor	~18	Not measured in literature but probably about hundreds
Number of turns	**Few**	**from 20 to 150**
Working frequency	**0.2 - 10 GHz**	**400 MHz**
Working temperature	4 K	few mK
Technology	CMOS for RF	custom
Track material	**Copper and/or aluminum**	**NbN or Nb**
Inductor type	rectangular/octagonal	Spiral

Inductors specifications inside LNA and qubit readout circuit

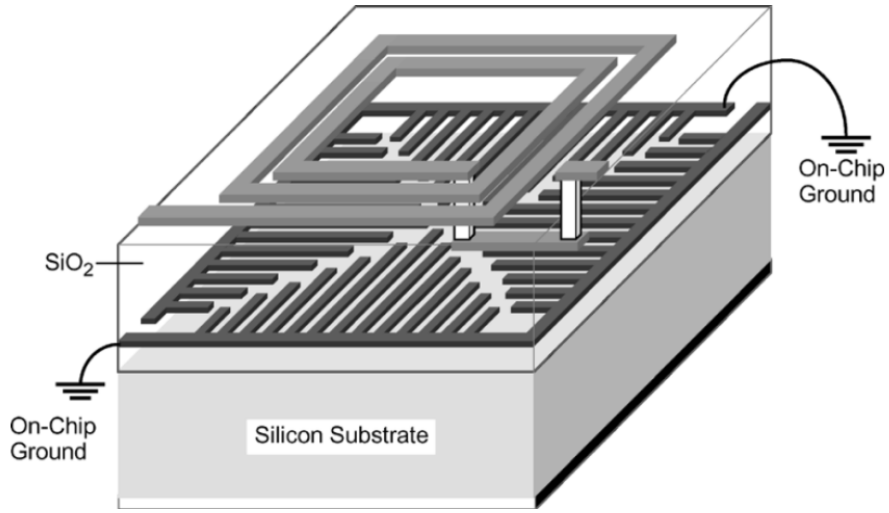
Objectives and problematic

How can the Q-factor and the intrinsic inductance of integrated inductor structures in 28 nm FD-SOI, be improved for use in qubit readout systems and RF applications?

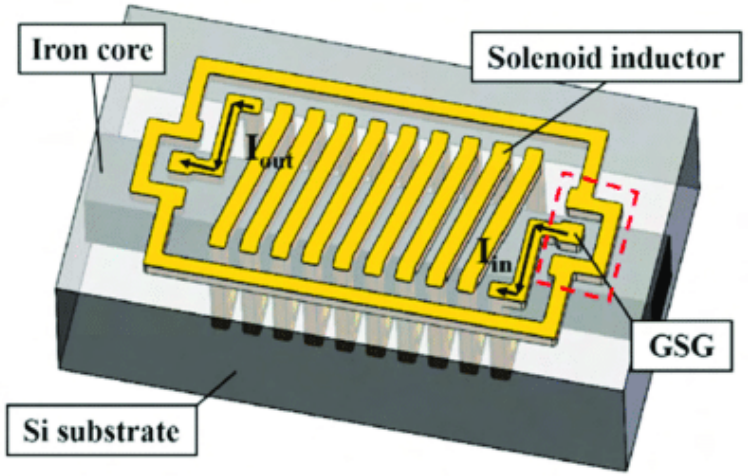
Selected paper of literature



Above IC



Shield at low metal level



Solenoid with a magnetic core

Solution to increase the quality of inductors

D. W. Lee and all, *IEEE Transactions on Magnetics*, [2008]
S. L. J. Gierkink, I*EEE Journal of Solid-State Circuits,* [2003]
T. S. D. Cheung and J. R. Long, *IEEE Journal of Solid-State Circuits*, [2006]

Levers for higher performance inductors

- Design and material used in inductor
- Using a shield to lower inductor-substrate interaction
- Adding soft magnetics materials
- Use above-IC method

EM Simulation

Simulation – inductor geometry

Ansys HFSS

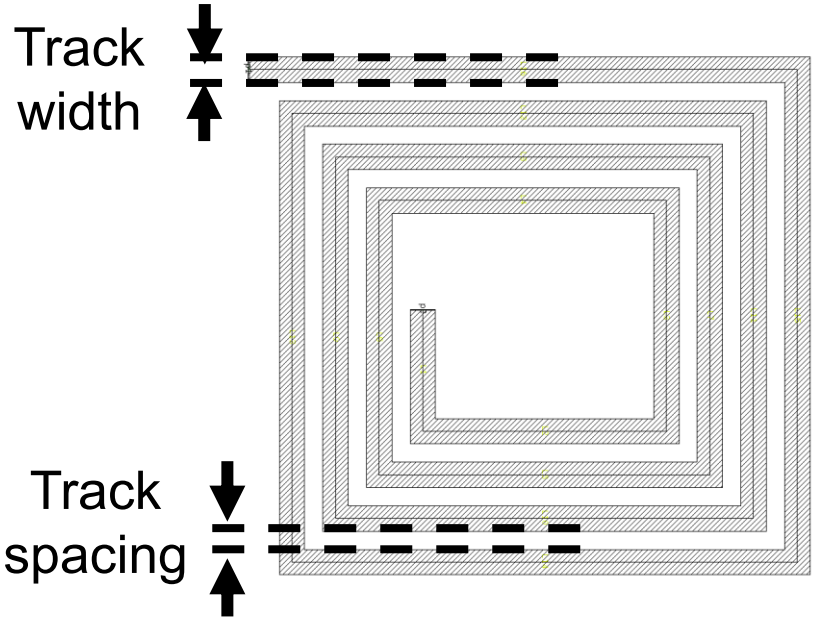
cadence Momentum

FAST (ST)

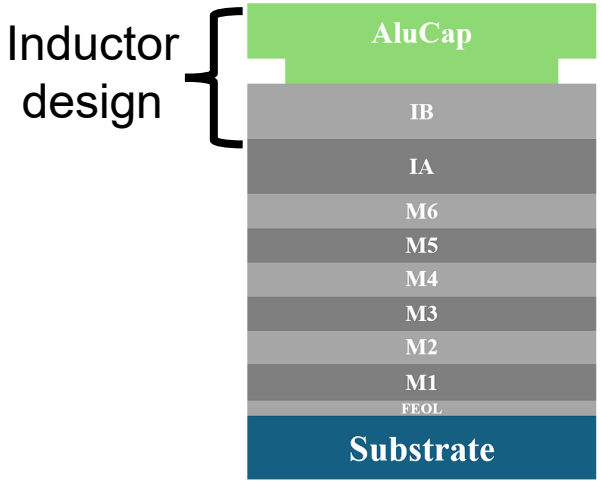
- 3D EM simulator: HFSS
- 2.5 D EM Simulators: Momentum and FAST
- Typical simulator for inductors

Quantifying the impact of the different identified levers

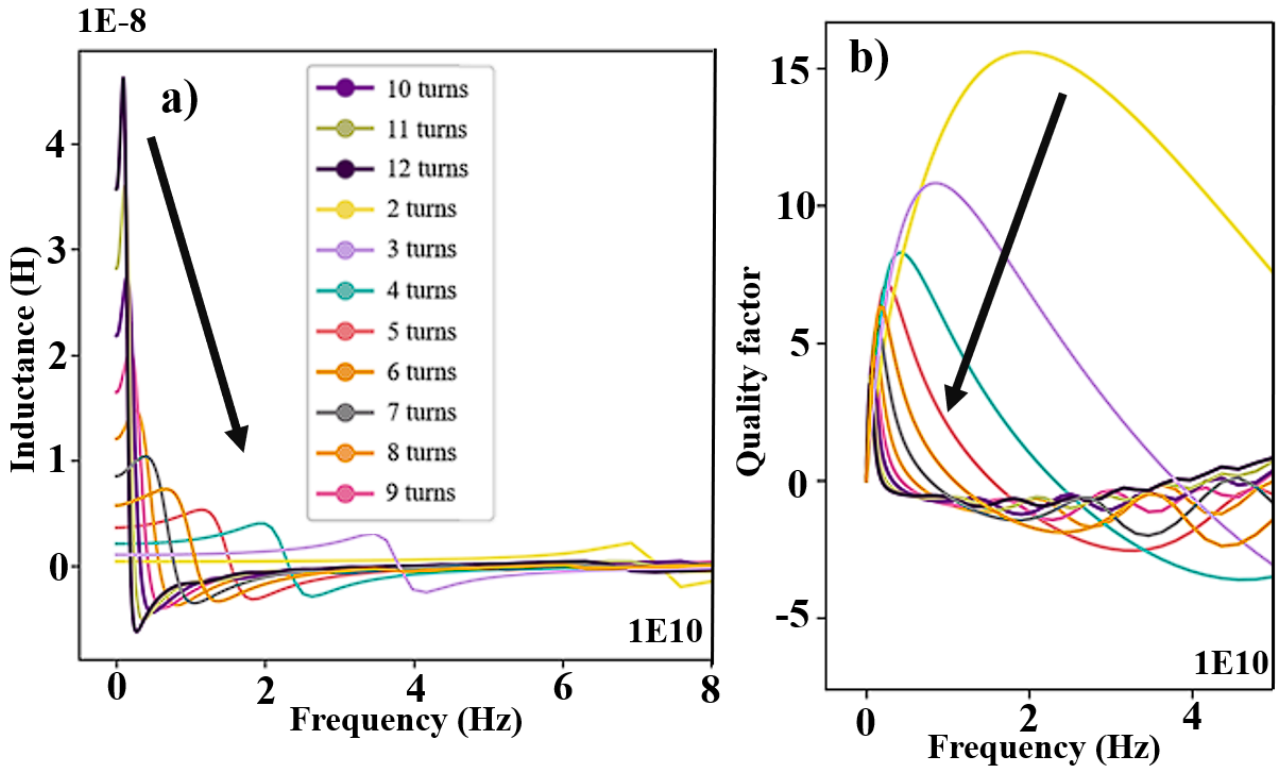
Simulation – inductor geometry



Metal stack:



Variation of number of turns:

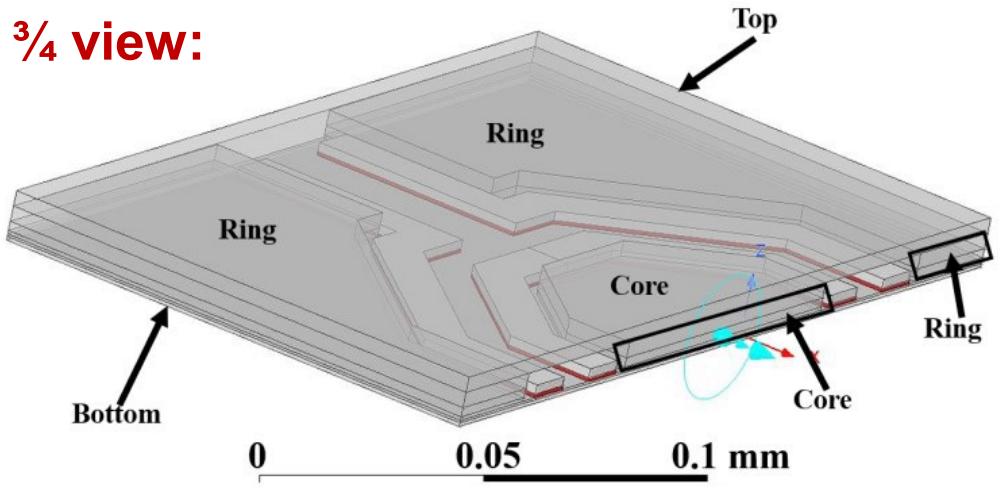


Geometry of the inductor balances inductance (L), quality factor (Q), and occupied area

With internal ST tool “FAST”

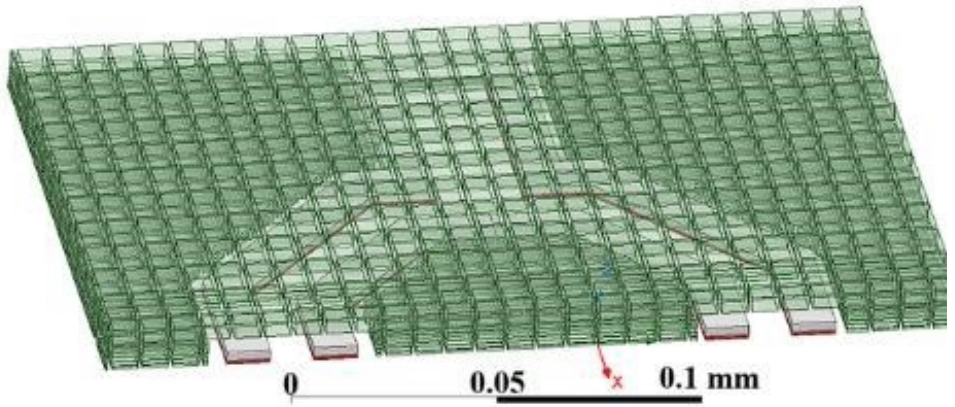
Simulation – investigation of 3D magnetic structures

¾ view:



Inductor with **unpatterned** magnetic material

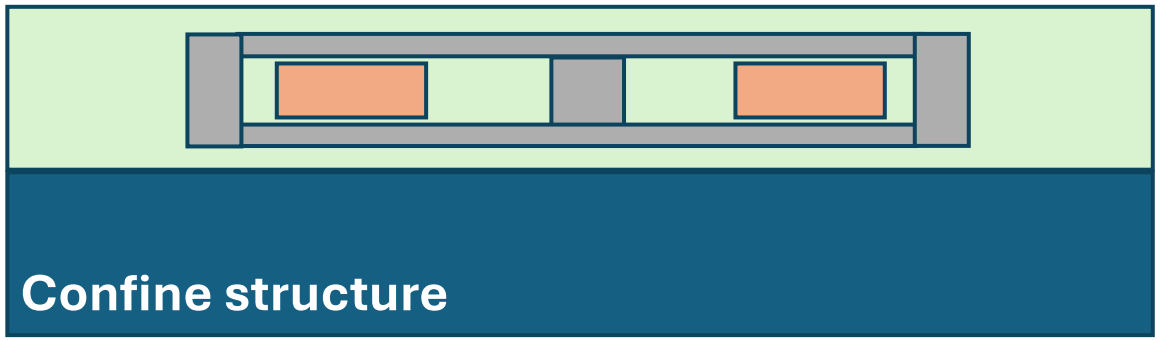
¾ view:



Inductor with **patterned** magnetic material

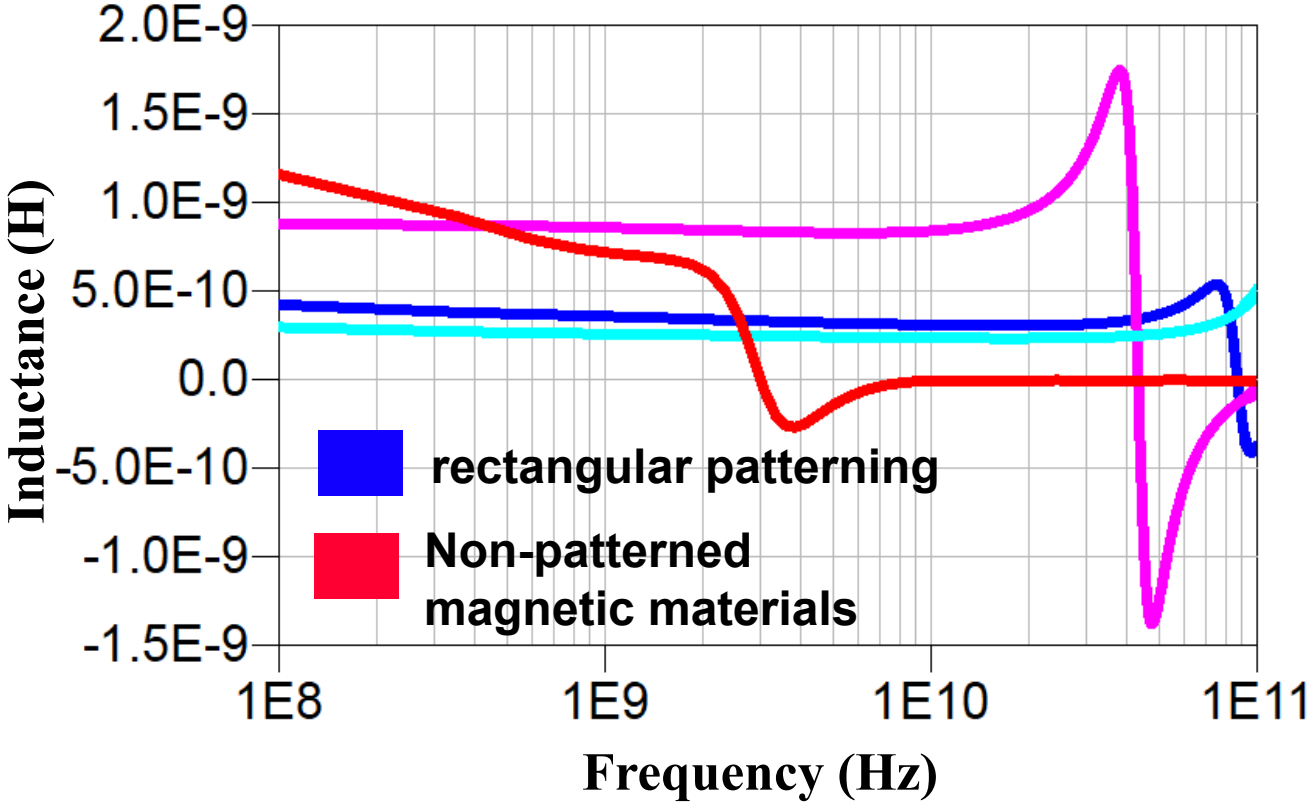
- Magnetic Materials
- Silicium dioxyde
- Silicon substrat
- Inductor track

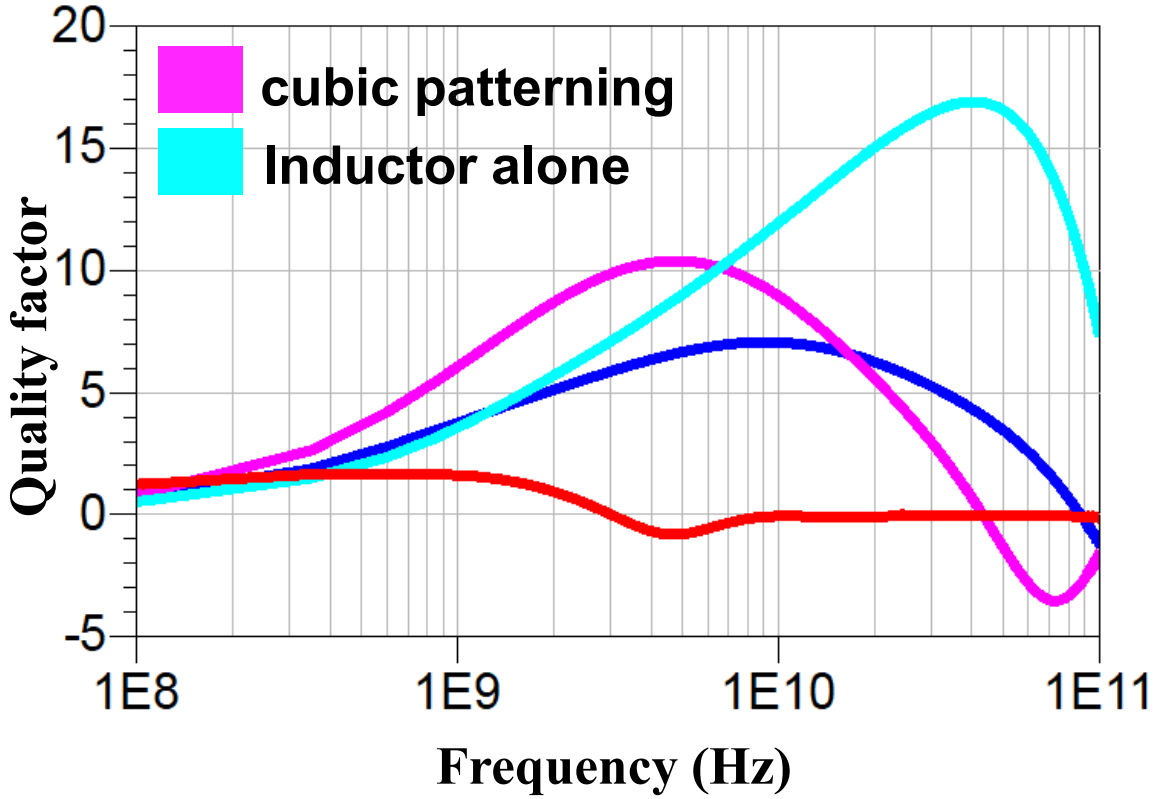
Cross section view:



Evaluation of magnetic material impact

Simulation – investigation of 3D magnetic structures

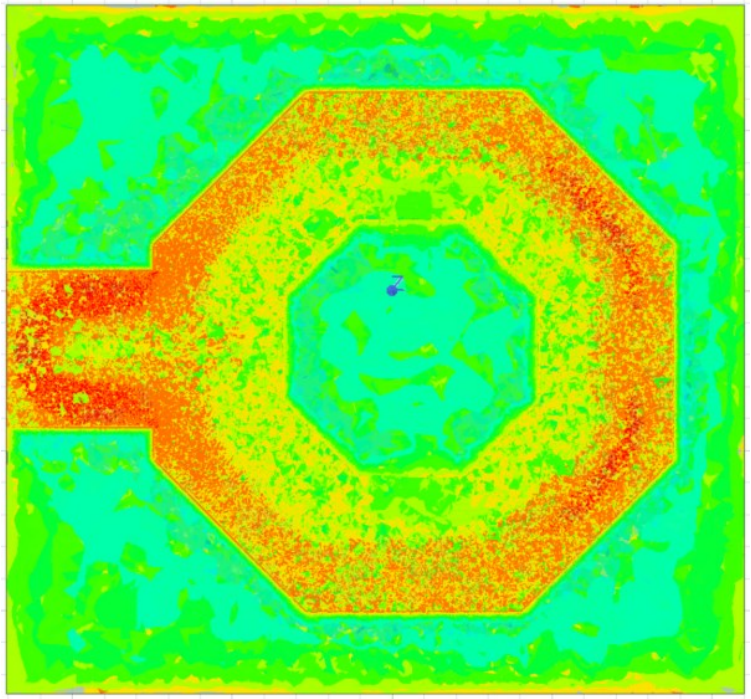




Soft magnetics material impacts the inductor performances

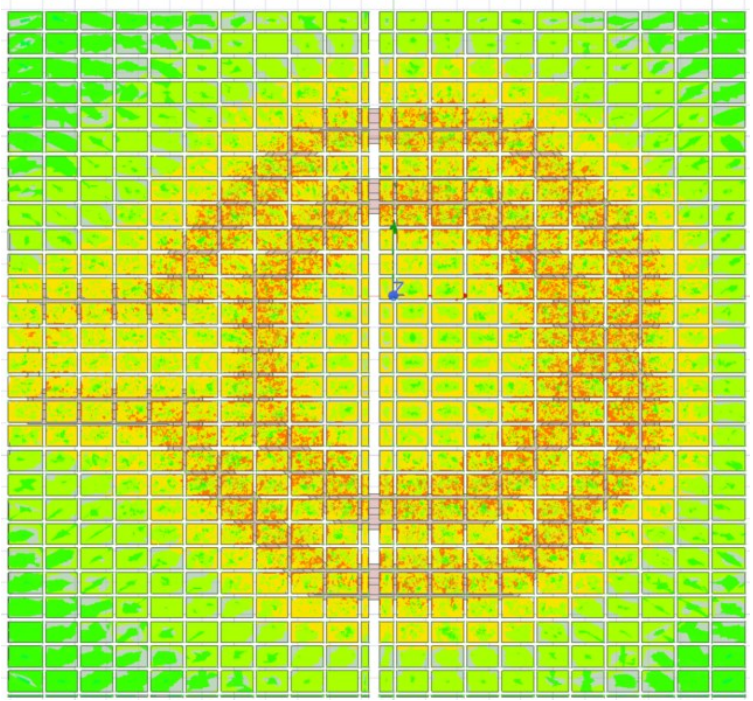
This study was done at **room temperature**

Simulation – investigation of 3D magnetic structures

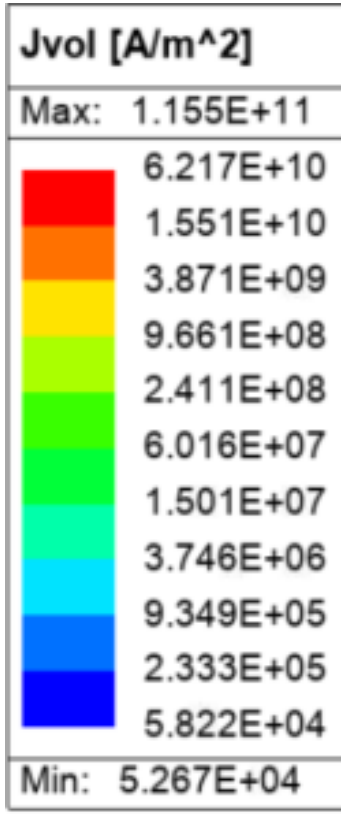


Plain magnetic material

At 7 GHz



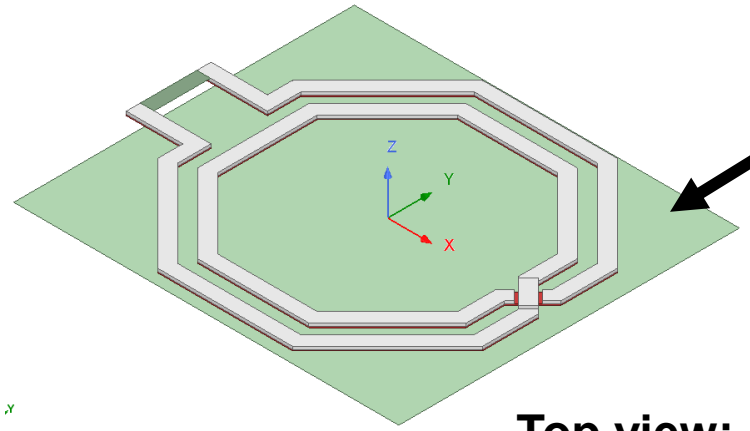
Cube patterned magnetic material

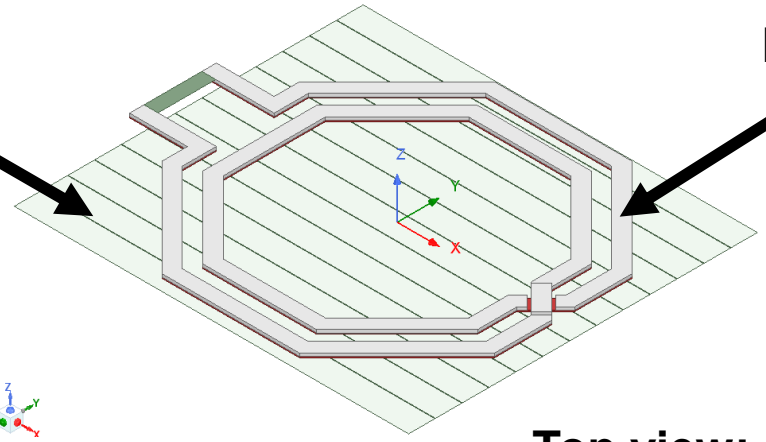


Soft magnetics material patterning impact Eddy current flowing

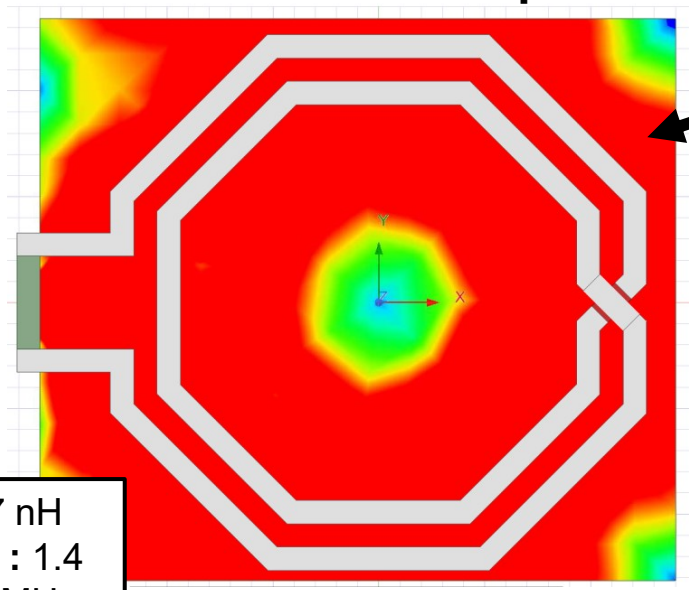
At room temperature

Simulation – Effect of metal shield addition





Top view:



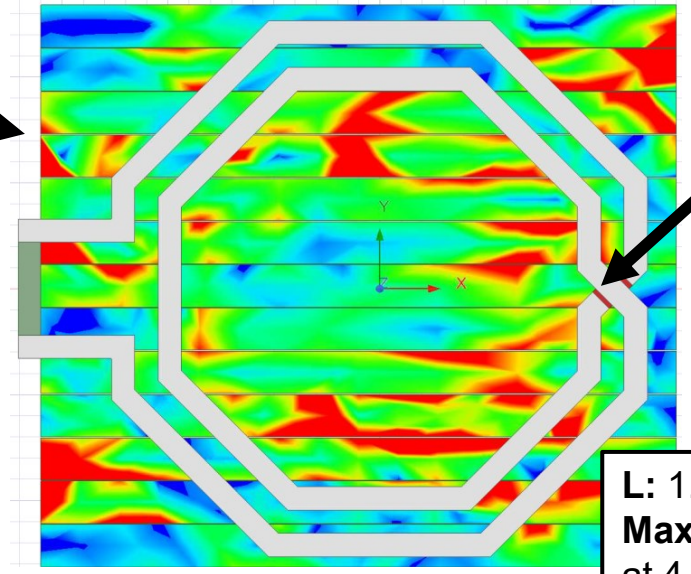
L: 1.07 nH
Max Q : 1.4
at 600 MHz

Strong current

Medium current

Low current

Top view:

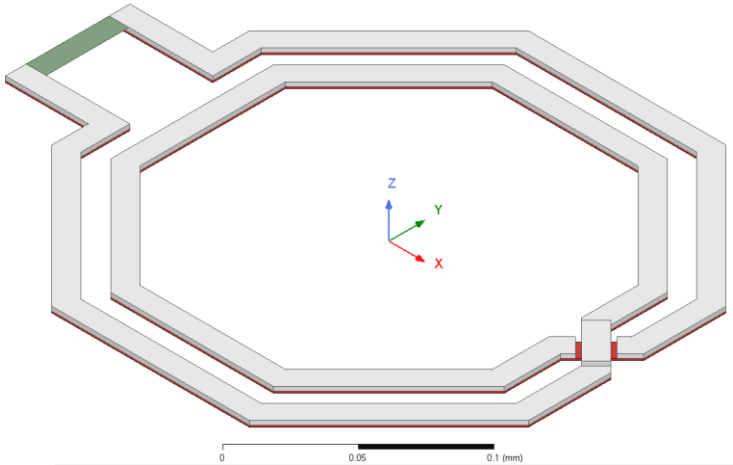


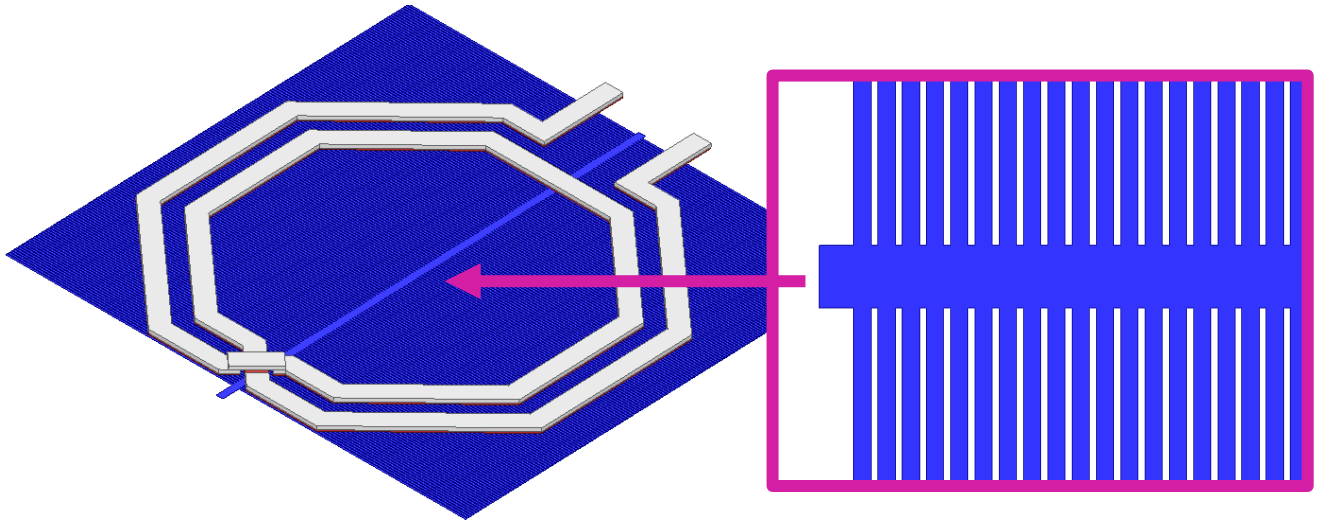
L: 1.38 nH
Max Q : 10.7
at 4.4 GHz

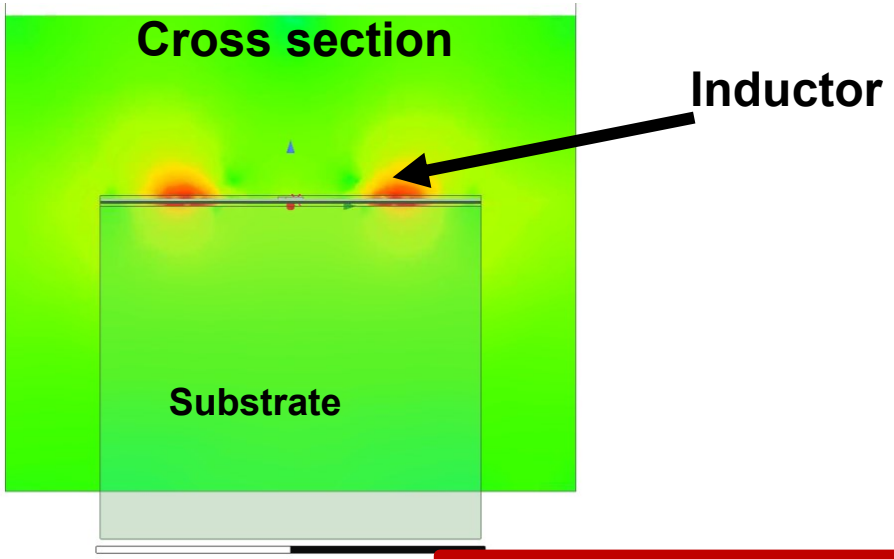
Controlling the current within the shield

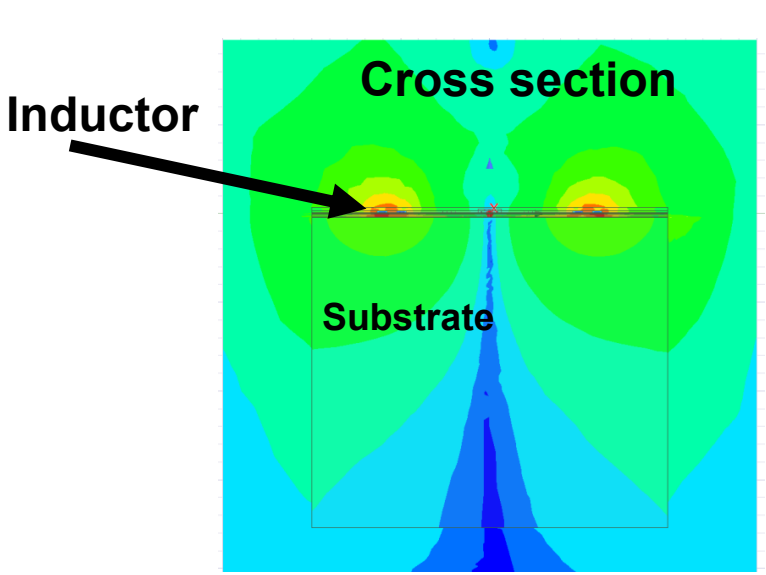
At room temperature

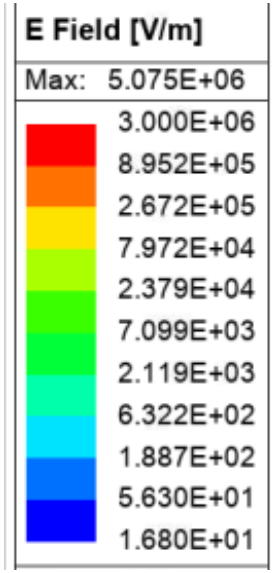
Simulation – Effect of metal shield addition







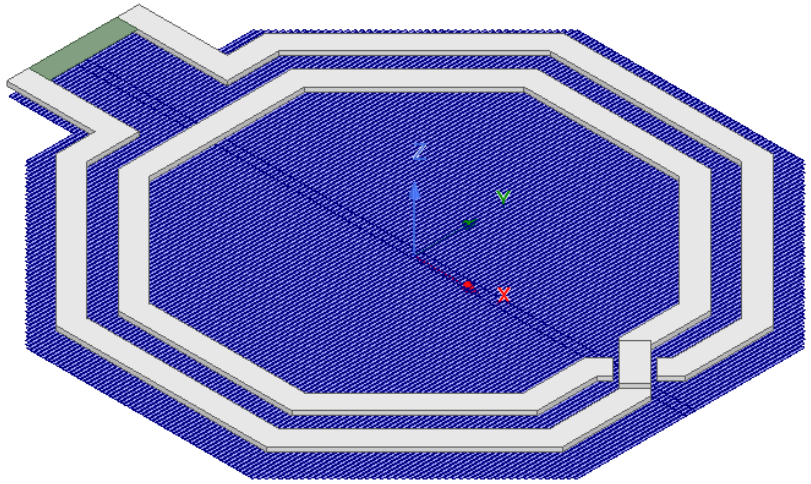


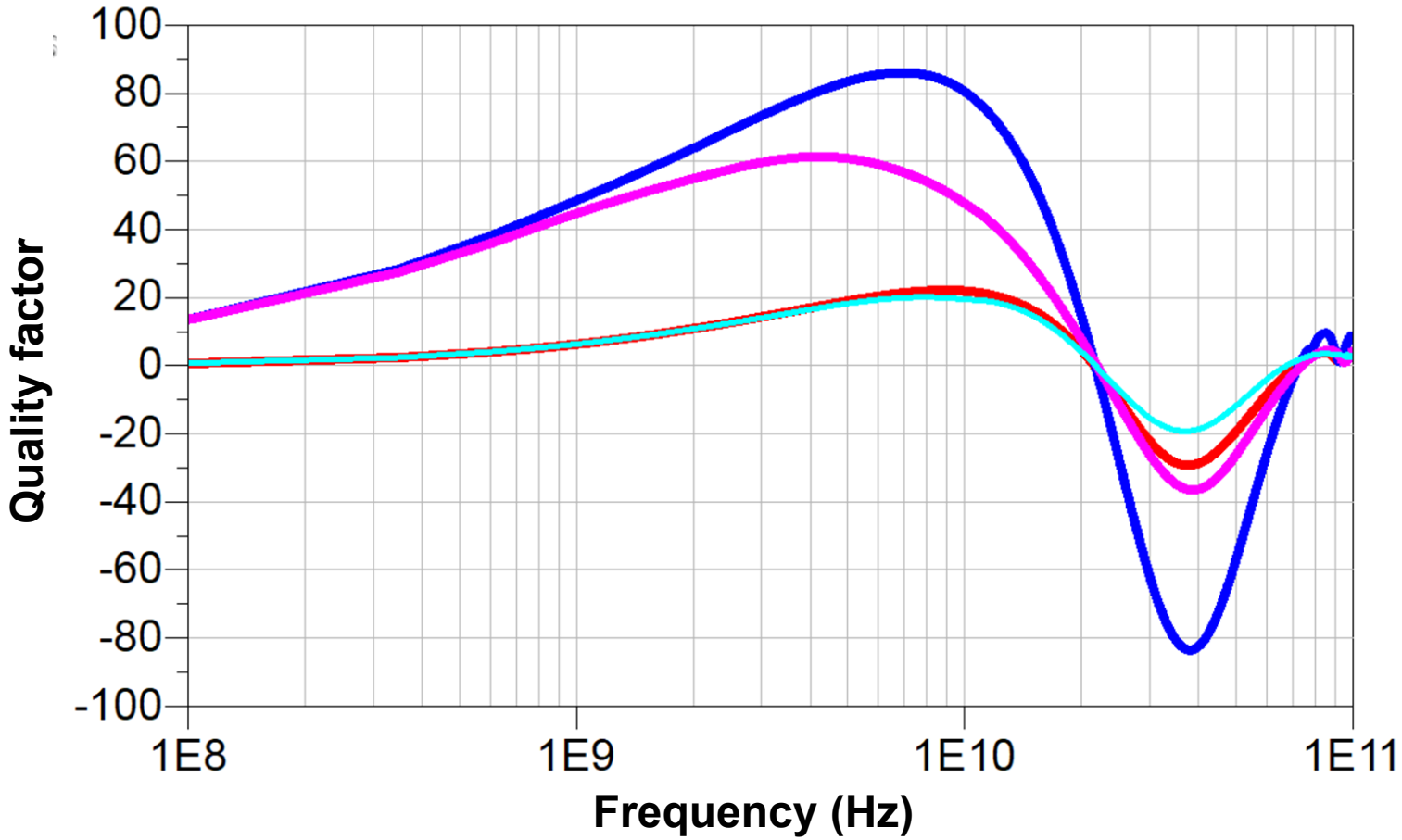


At room temperature

Controlling inductor-substrate interaction

Simulation – Effect of cryogenics temperatures





Classical Inductor

Inductor with Cryogenic Track

Inductor with Cryogenic Track and Shield

Inductor with Cryogenic Shield

At 4 K

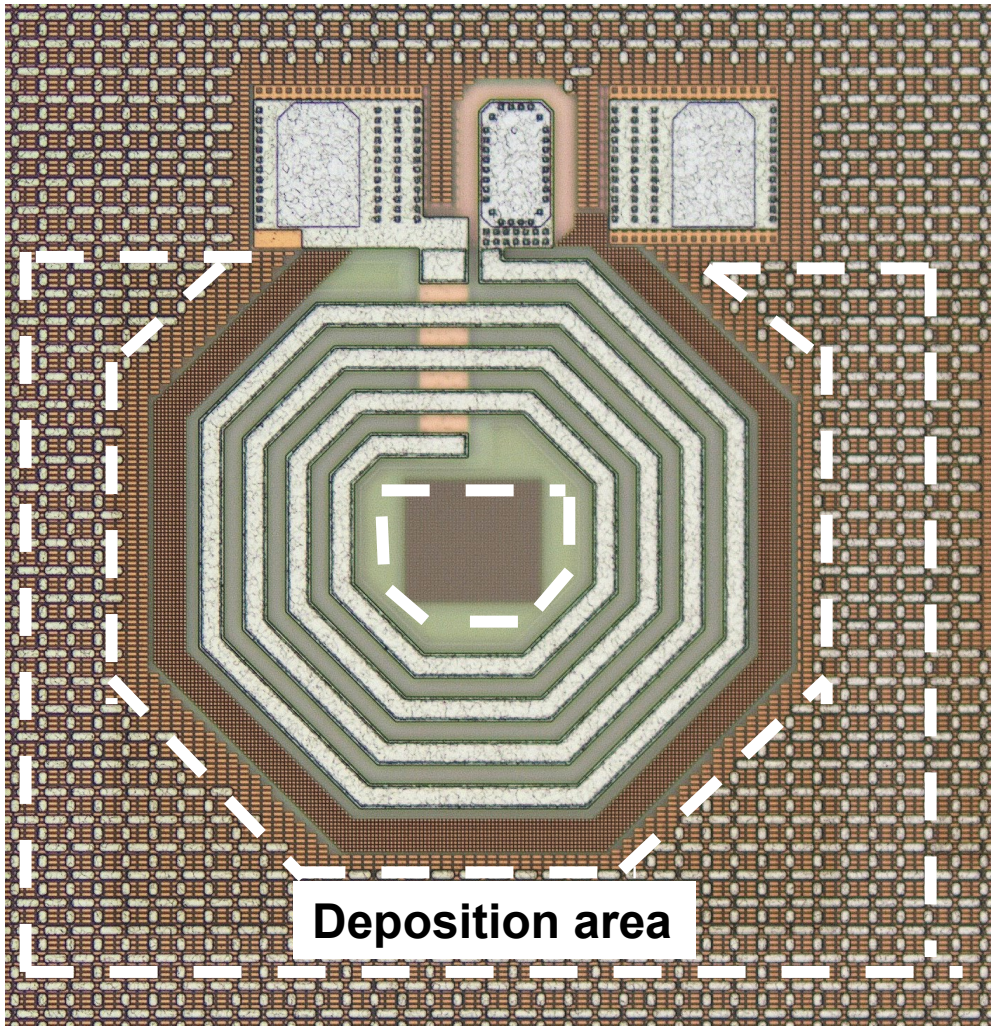
Increasing inductor quality by lowering temperature

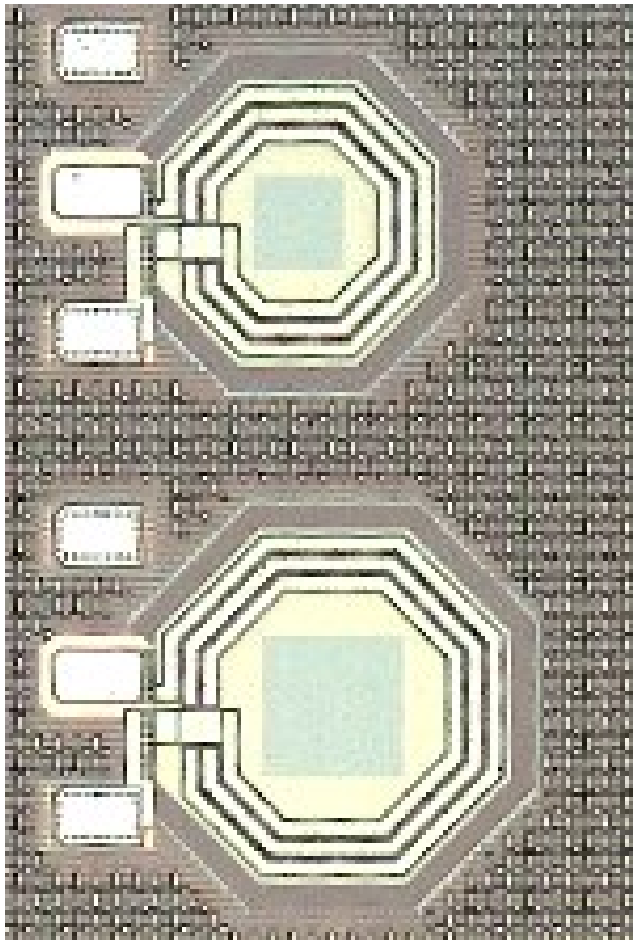
Simulation - conclusion

- Inductor geometry influence the performances
- A wide chosen shield shape could enhance the quality factor
- Magnetic material could enhance the inductance but lower the quality factor
- Choosing high conductivity material for inductor’s track increase the quality factor

Deposition Process of NiFe

Deposition of NiFe – ST Inductor set



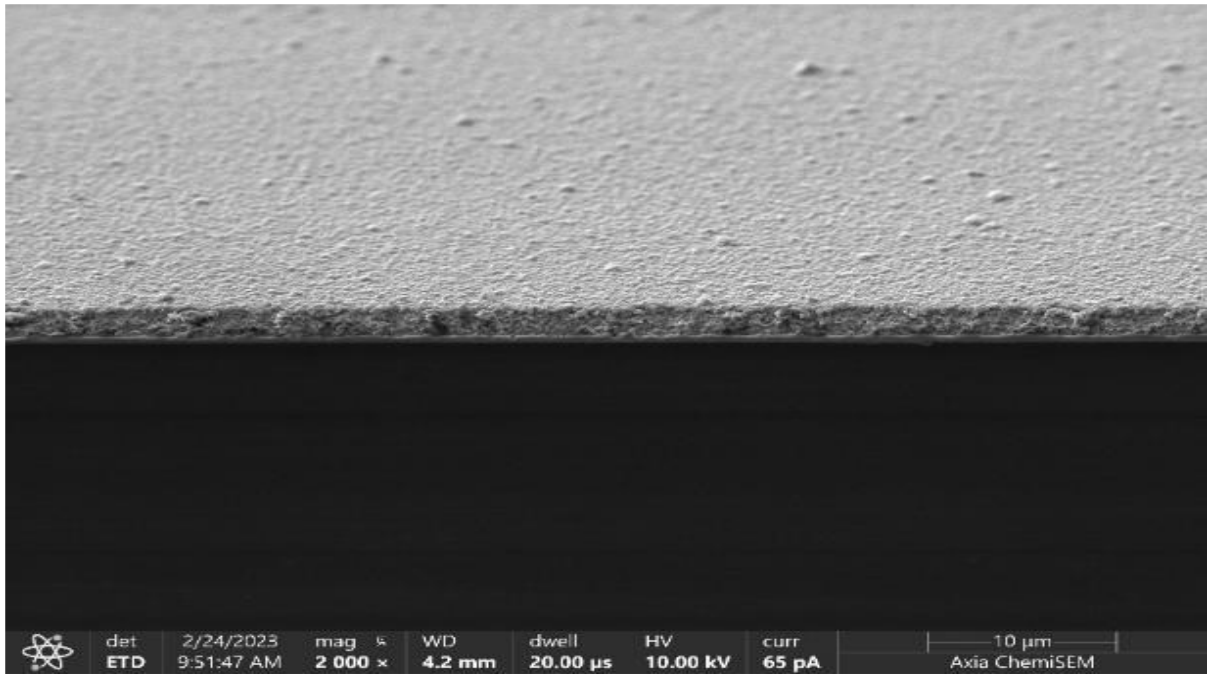


- Spiral inductors
- 2 inductors geometries
- 2 to 5 turns
- For RF application
- Reuse of NiFe
- 65 nm SOI mmW
- Process development done at 3IT (Sherbrooke)

Deposition area identification

Deposition of NiFe – Soft Magnetic Material deposition

- Chosen magnetics material: Ni45Fe55
- Electrical resistivity: 40 μΩ.cm
- Seed layer: 30 nm Titanium / 100 nm copper

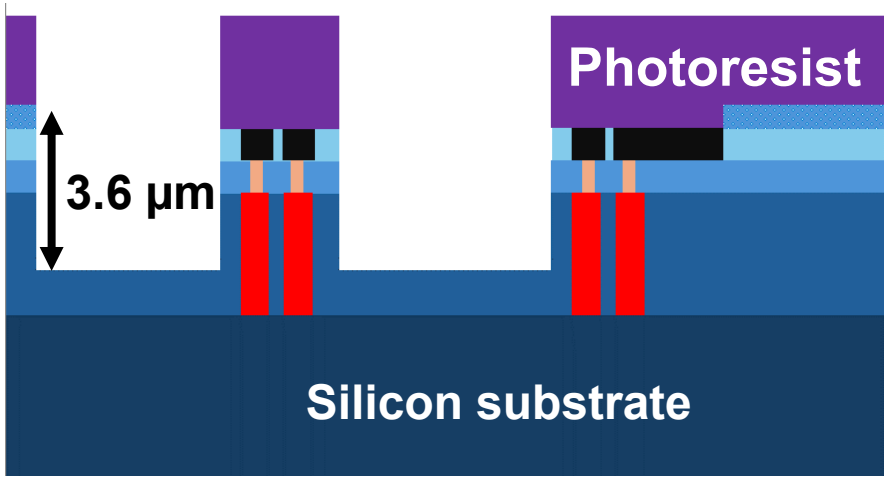


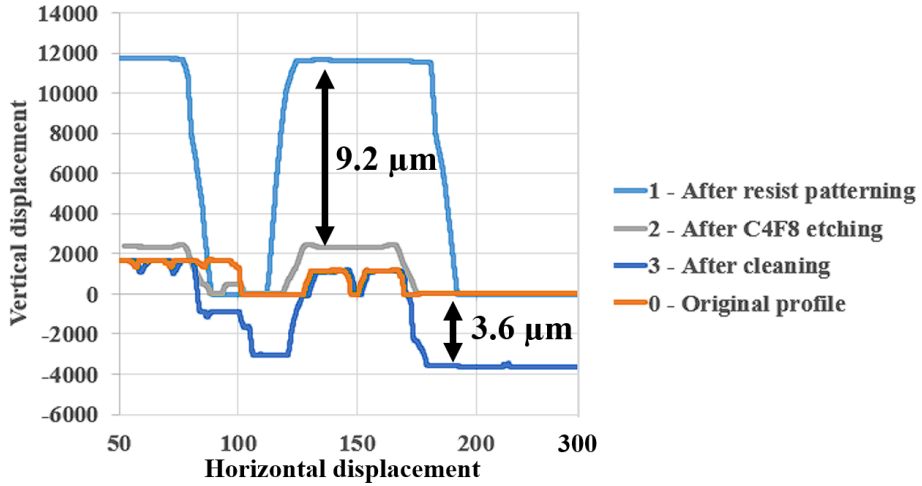
NiFe is compliant with literature

Deposition of NiFe – Established process

Process flow:

- Mask alignment
- Patterning photoresist
- C4F8 etching
- O2 Cleaning
- Ti/Cu Blanket Deposition
- Resist patterning
- NiFe Deposition
- Ion milling

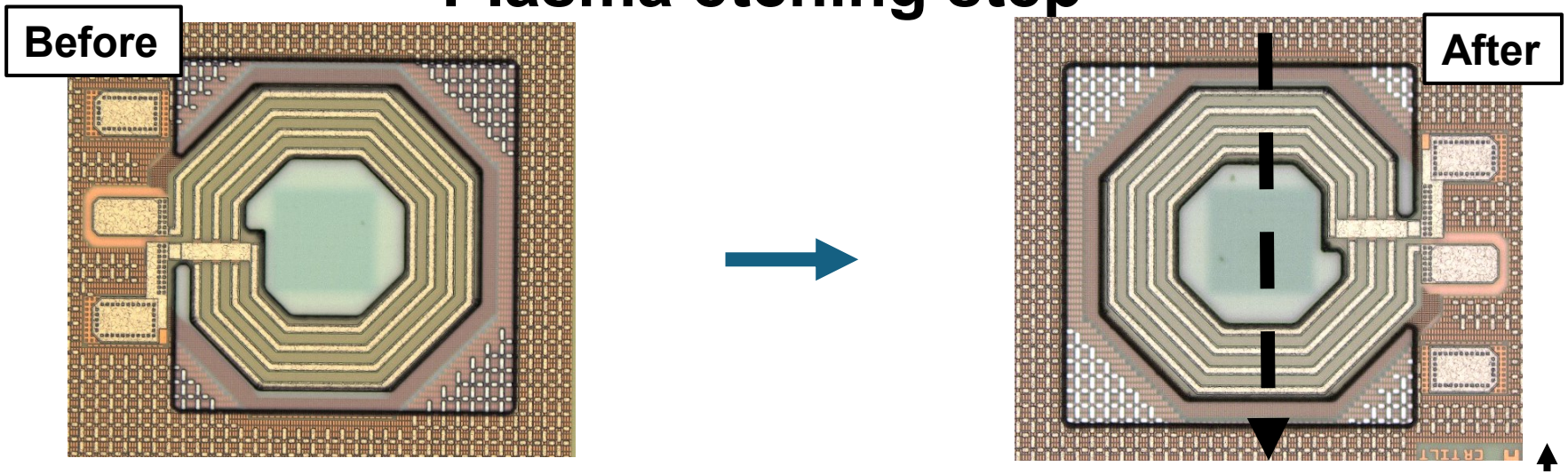




Plasma etching step

Legend:

- Aluminum layer
- Copper layer
- Silicon dioxides



Profilometer tip:

3.5 µm were etched by C4F8

Deposition of NiFe – Established process

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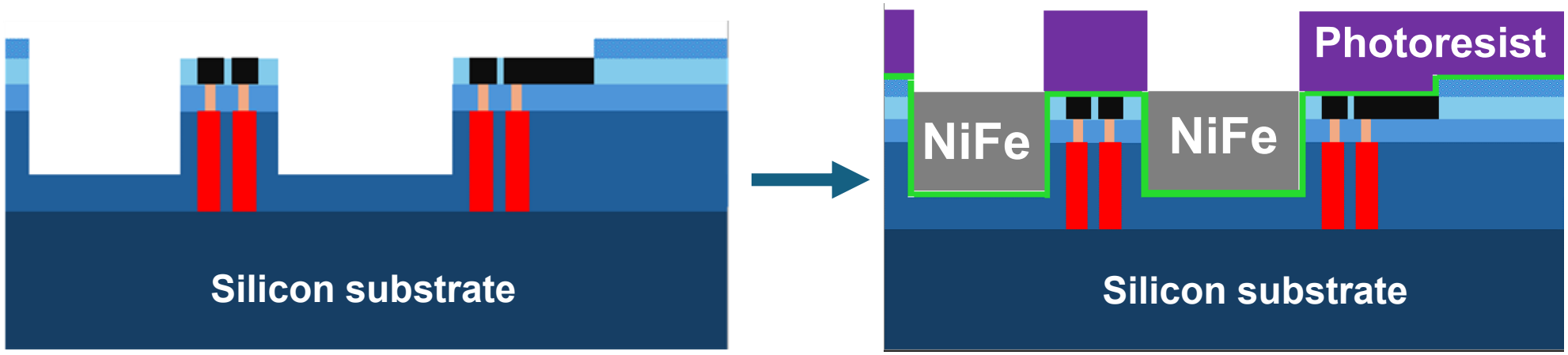
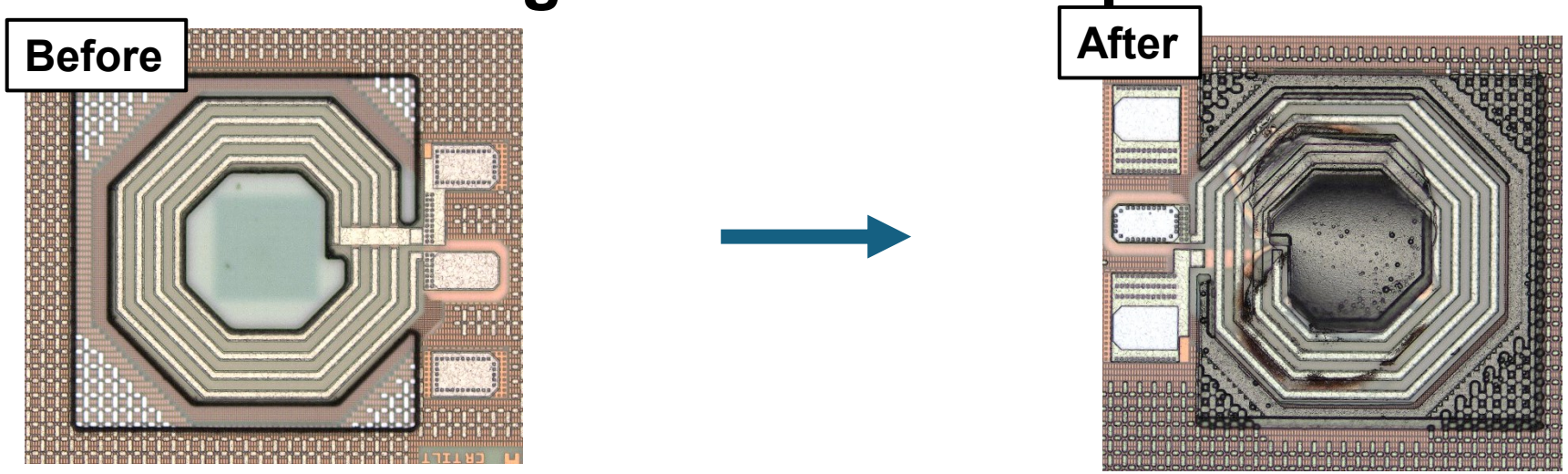


Soft magnetic material deposition

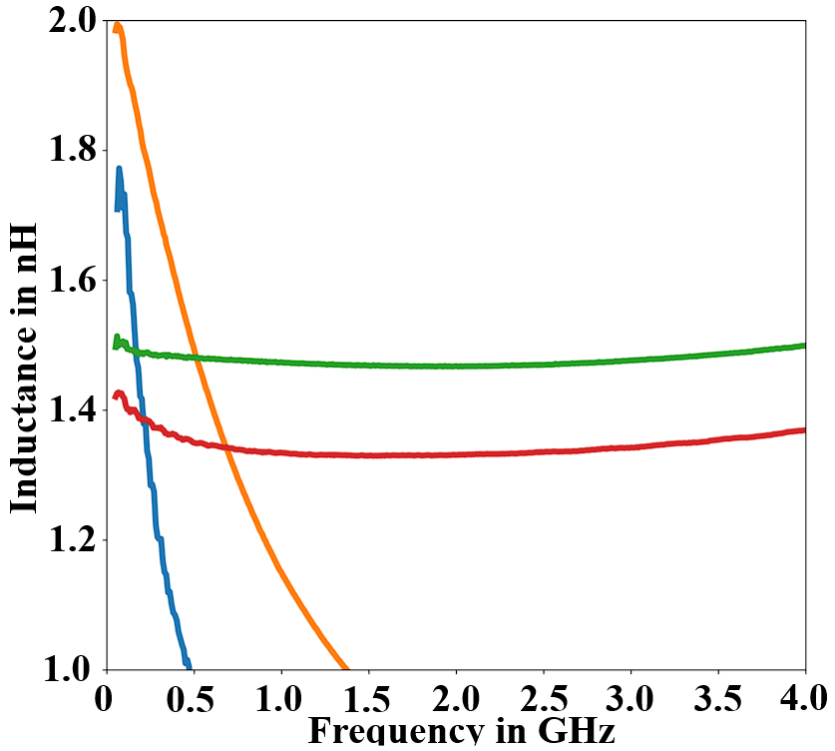


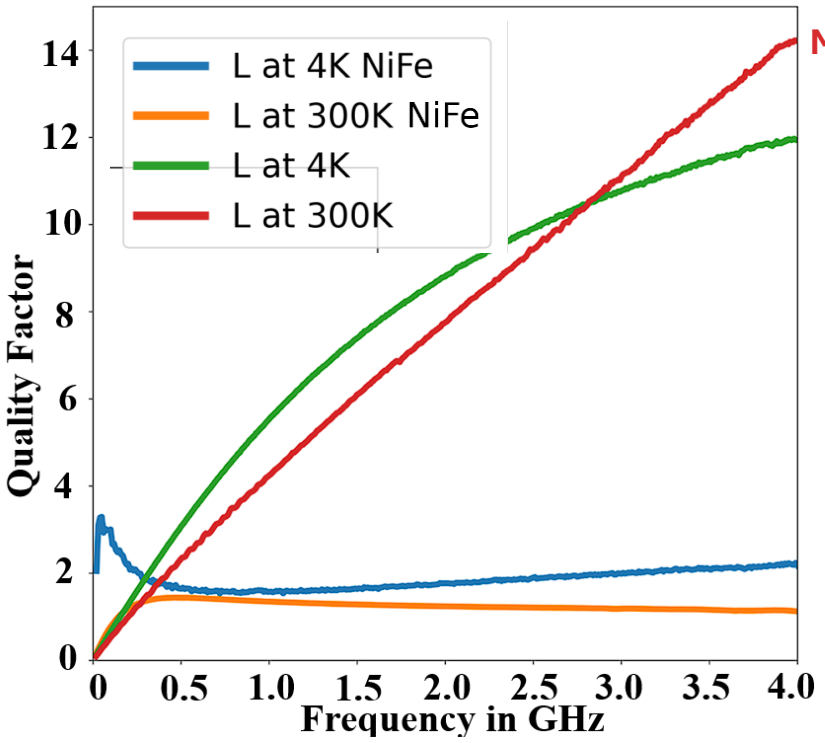
NiFe was successfully deposed around the inductor

Measurements

Deposition of NiFe – Temperature variation

Unpatterned NiFe was used in this work.



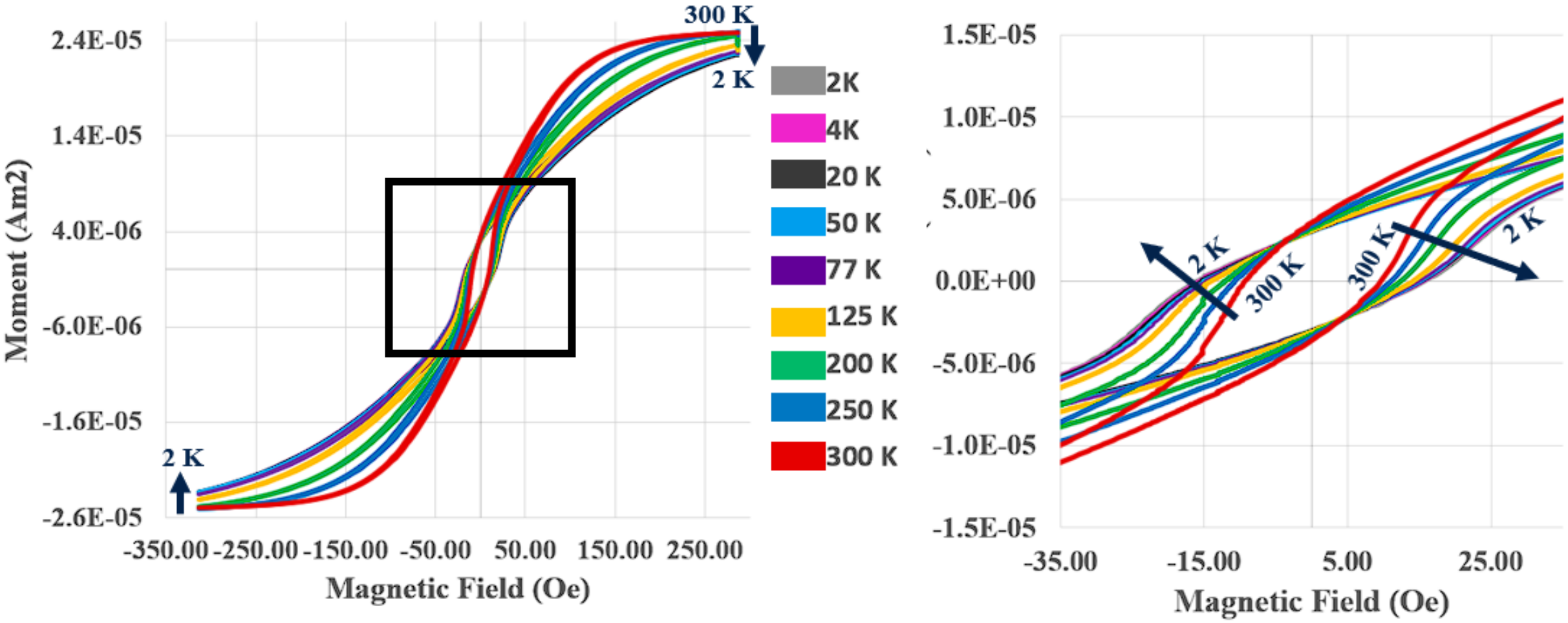


Max Q: 28

Max Q: 13

Visible gain in quality associated with track conductivity incensement

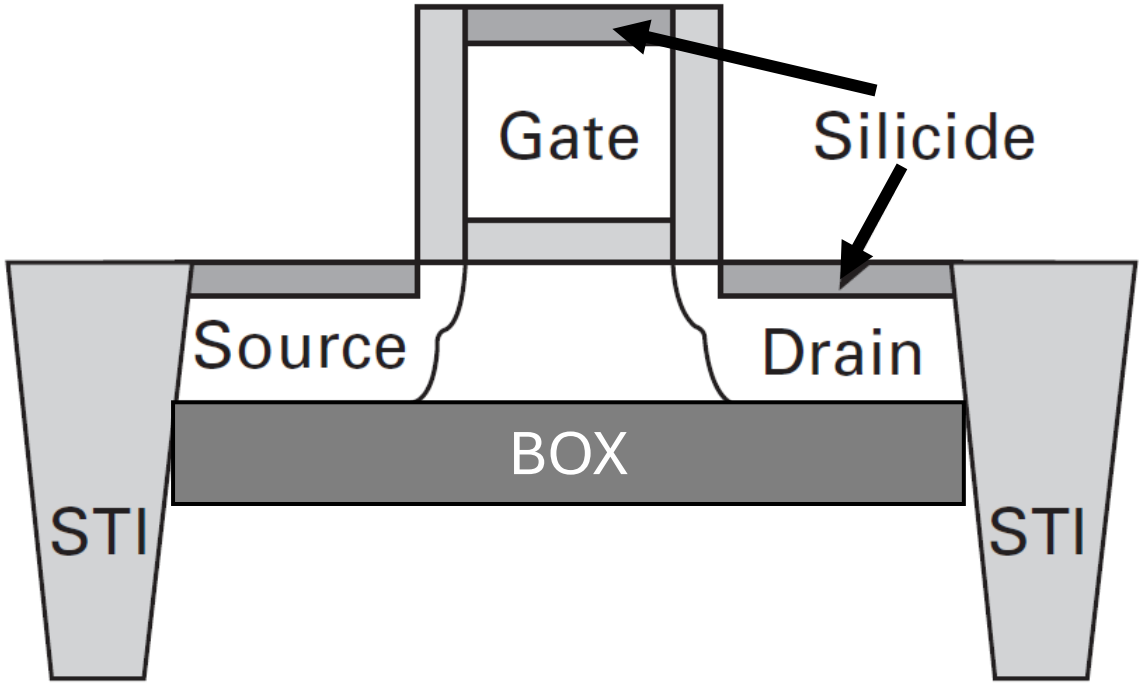
NiFe characterization – 300 K vs 2 K



Increasing of losses inside NiFe at 4 K

CMOS Silicides

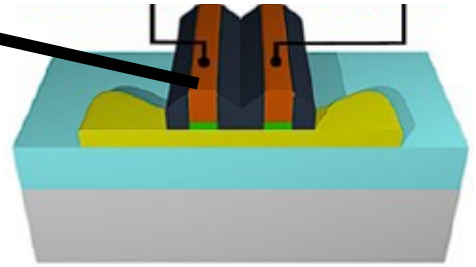
Silicides in CMOS



Cross section of FD-SOI transistor

Silicide typically used in semiconductor:

- TiSi2
- **CoSi2**
- NiSi

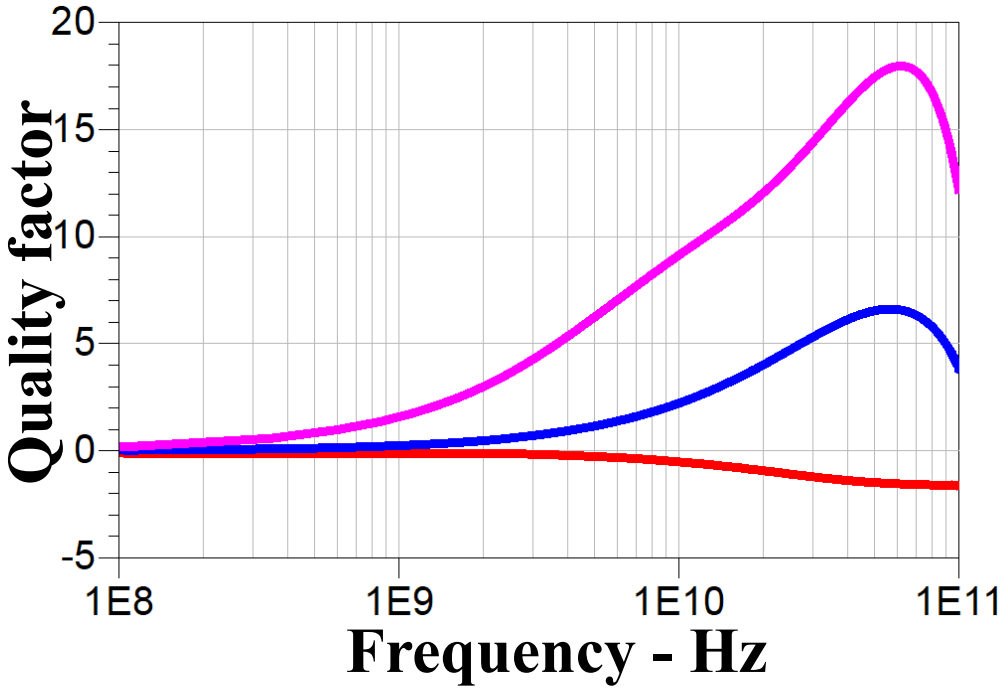


Quantum dot

Superconducting silicides can be used for rooting

S.-L. Zhang and Z. Zhang, *Structure, Processing and Properties*, [2014]

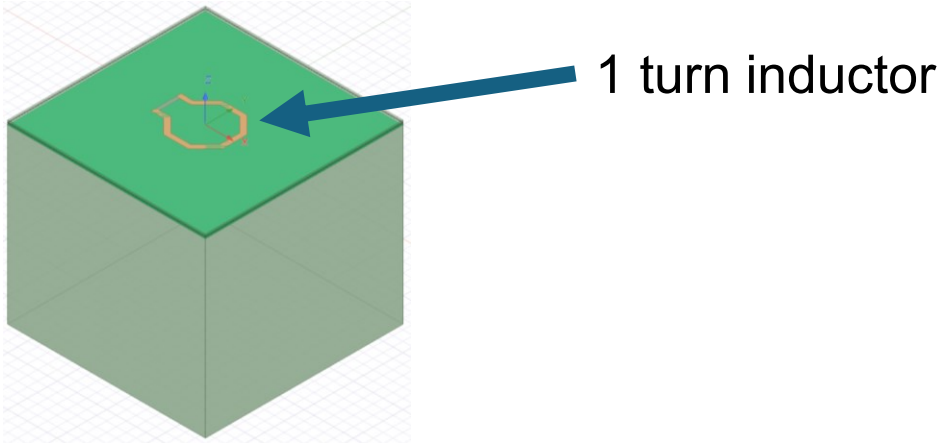
Silicides in CMOS

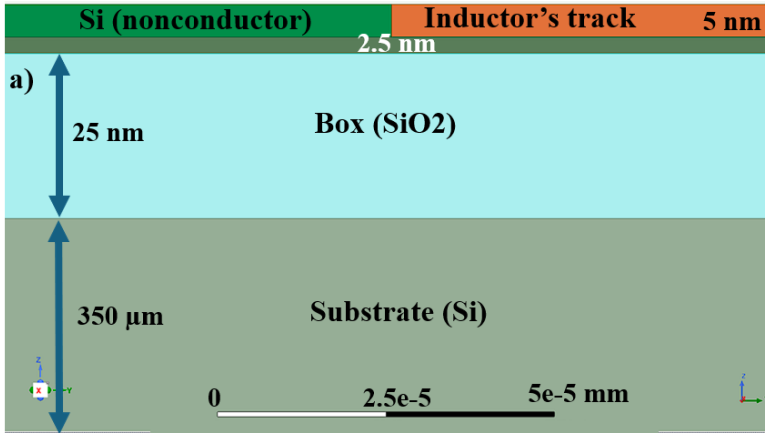


Silicide inductor – normal conductivity (room temperature)

Silicide inductor – conductivity x300 (cryo)

Silicide inductor – conductivity x2000 (cryo)

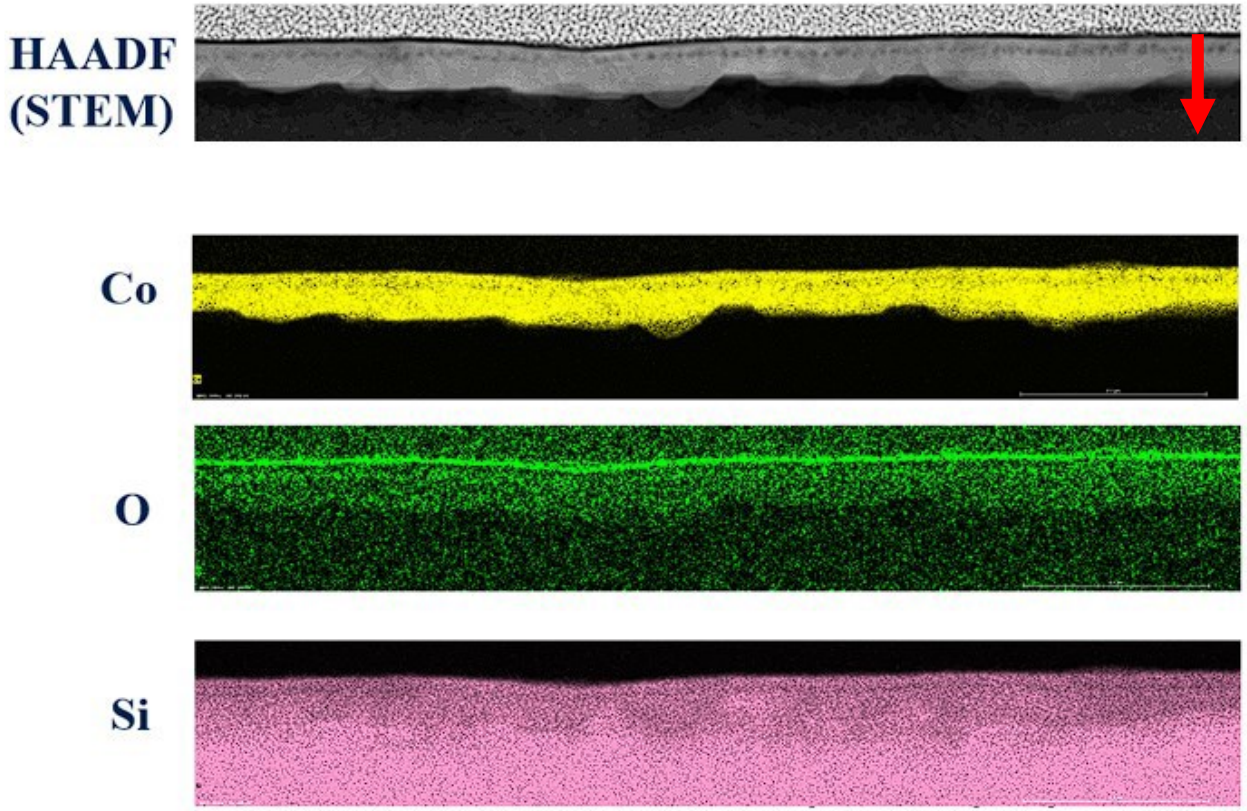




Cross section of simulated structure

Simulation show an increase of the quality of inductor with the track's conductivity

Silicides in CMOS

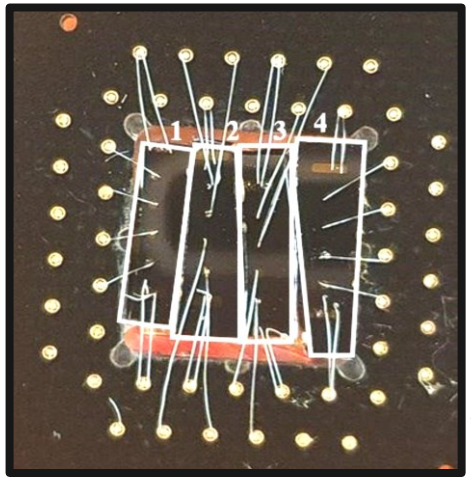


- Materials repartition (top to bottom):
- Oxygen thin layer
- Silicon
- Silicides formed using CMOS ST process

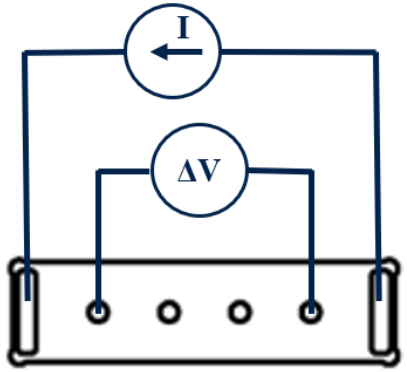
life.augmented

Characterization of deposed silicides

Measurement – sample preparations and experimental setup

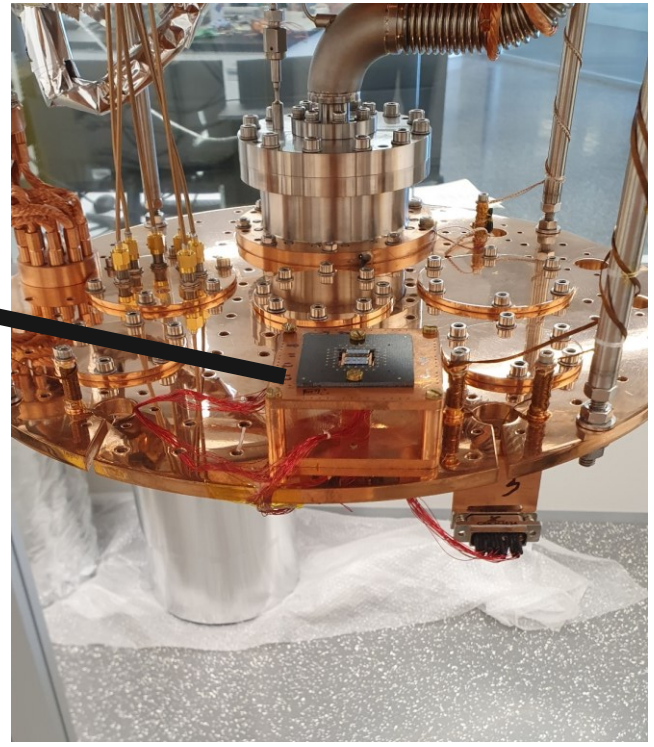


4 silicides on the sample holder



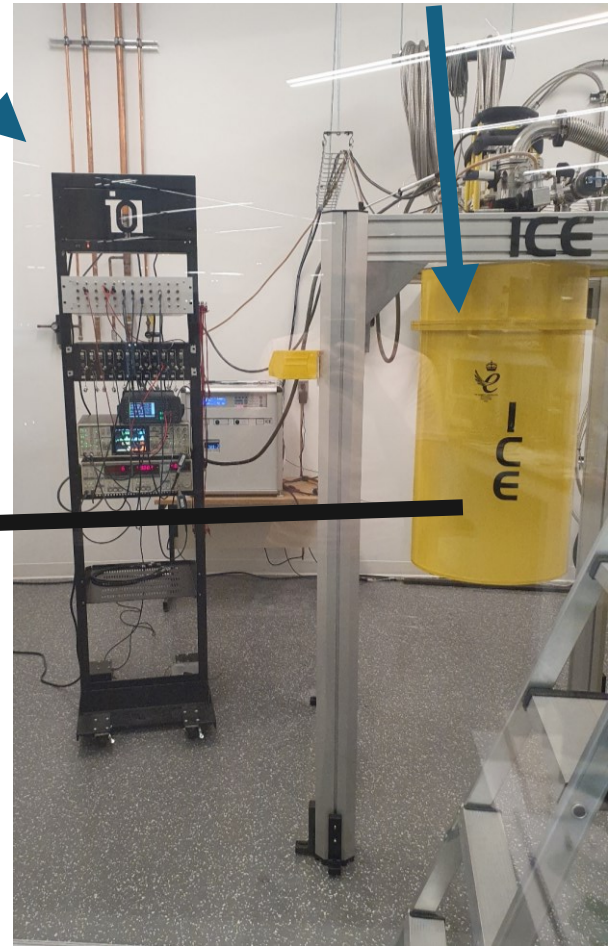
Four terminals measurement method

Ti/Au



Measurement unit

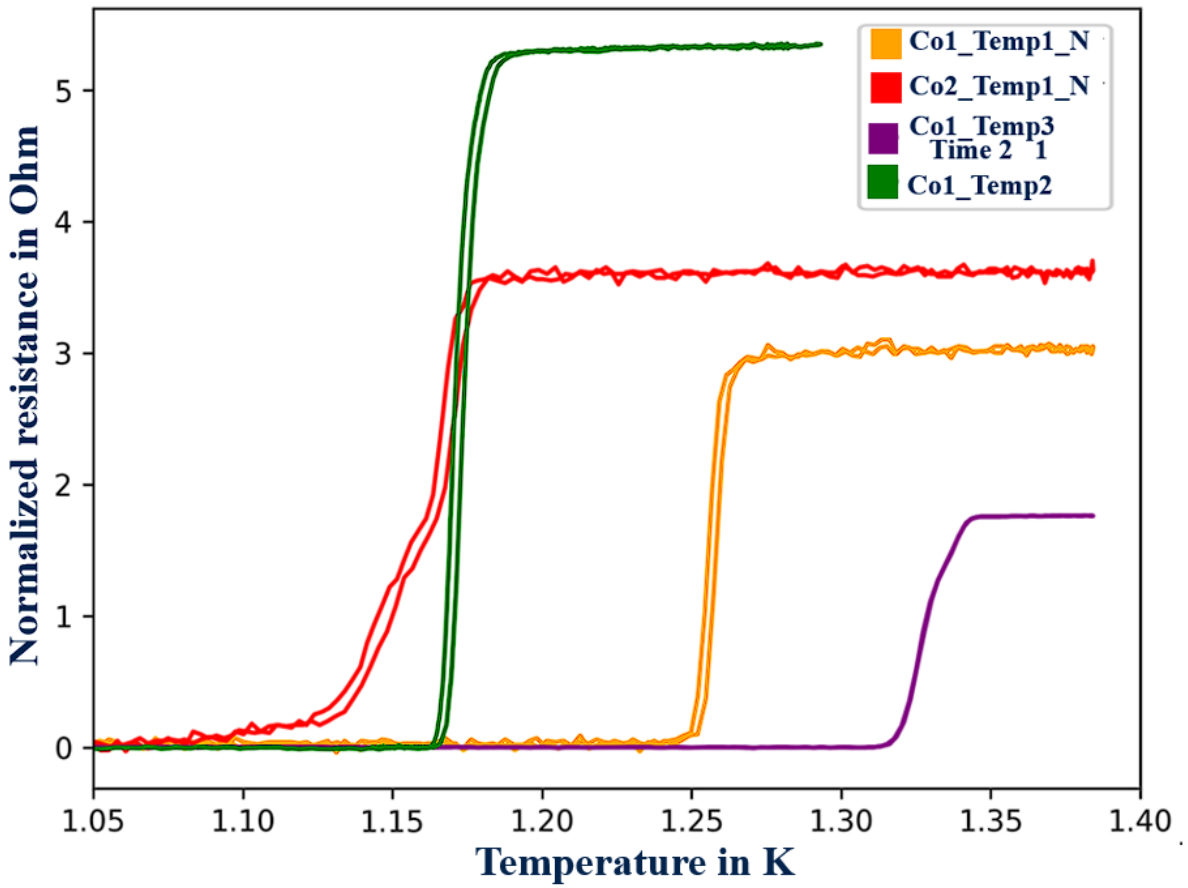
Ice oxford Cryostat

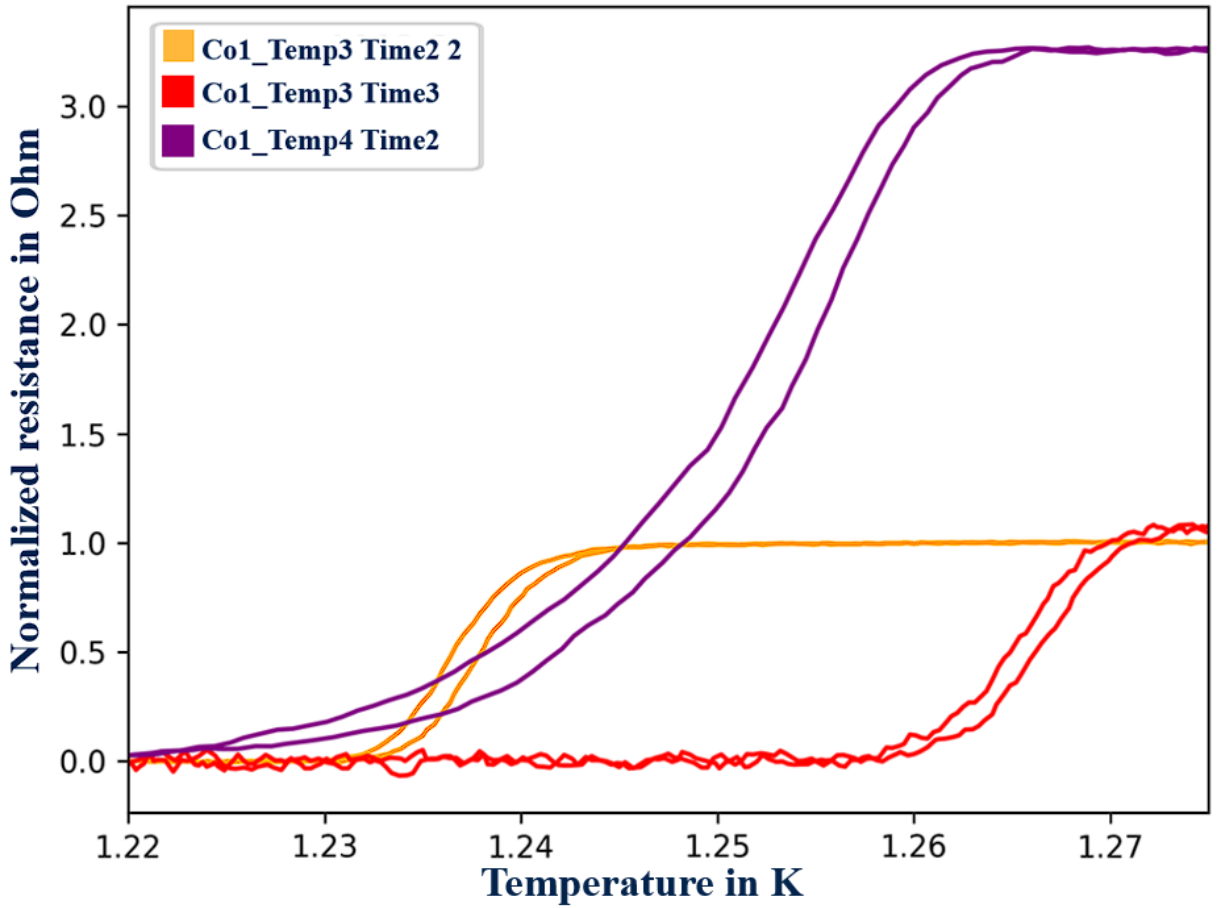


Measurement until 0.95 K

Using four terminal measurement method

Tc Measurement - results





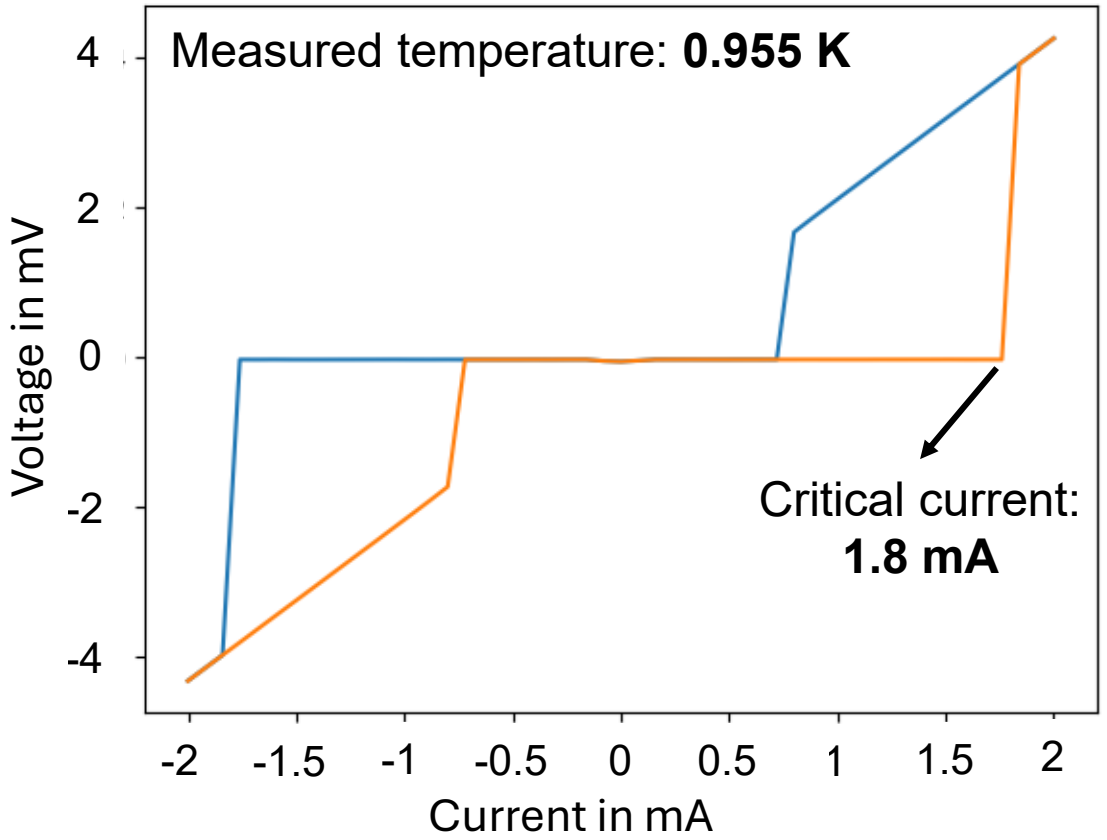
Critical temperatures has been identified in the range 1.10K to 1.33K

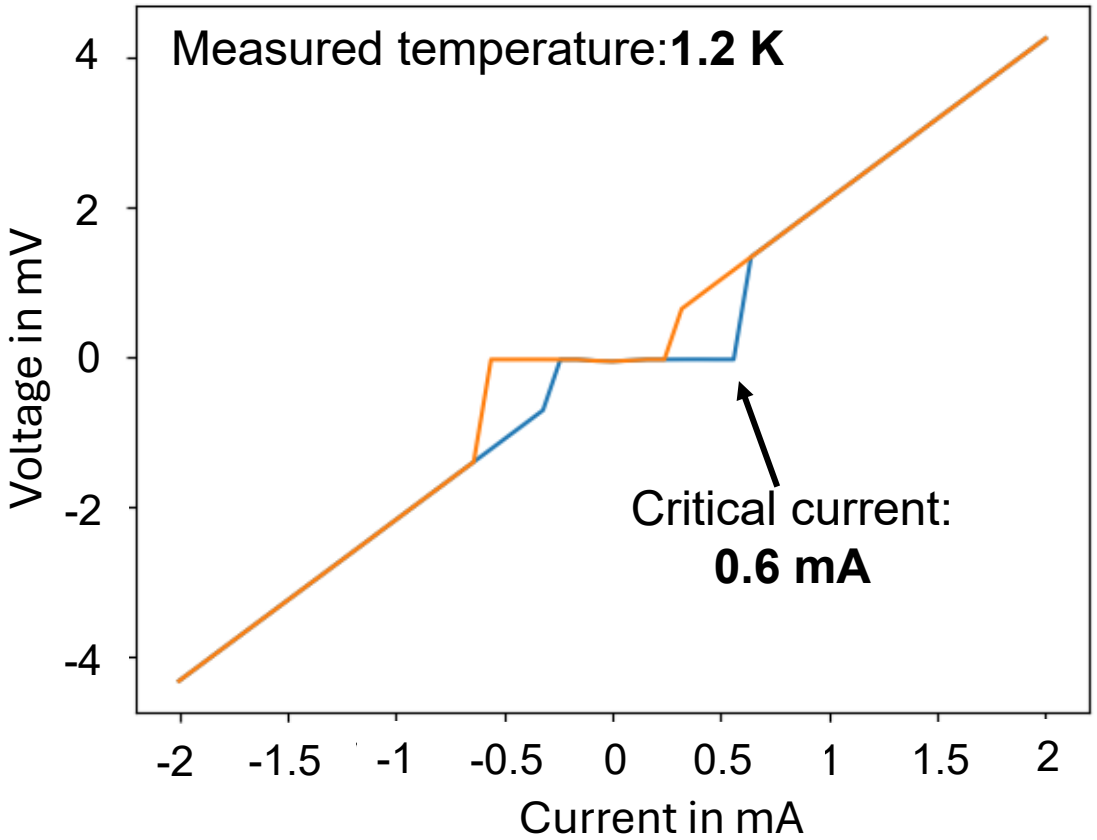
No external magnetic field applied

Critical current Measurements - results

Critical currents measured at : 0.955 K/ 0.99 K/ 1 K/ 1.105 K/ 1.1 K/ 1.15 K/ 1.2 K

Identified critical temperature : **1.33 K**



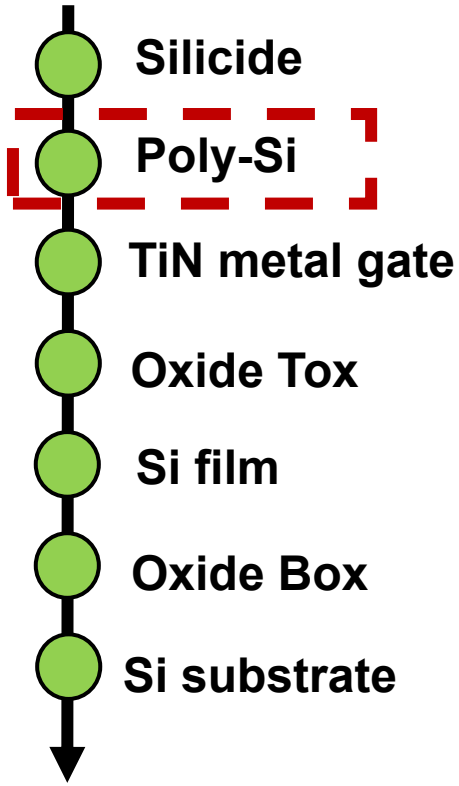


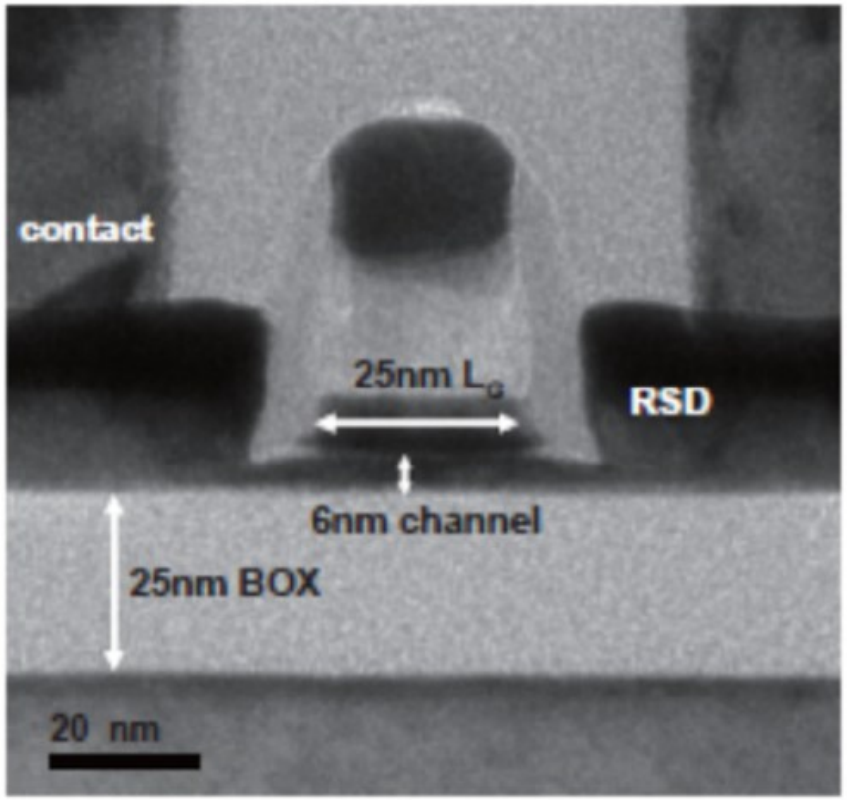
No external magnetic field applied

New device proposal

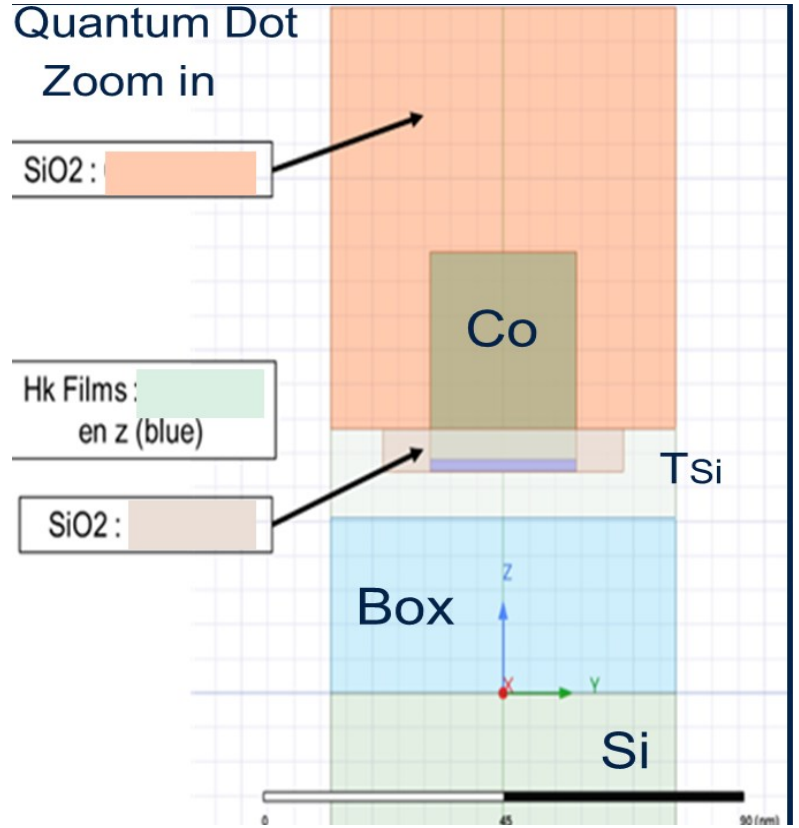
New device proposal – Transistor with magnetic gate

Gate metal stack:





SEM view of 25 nm UTBB transistor



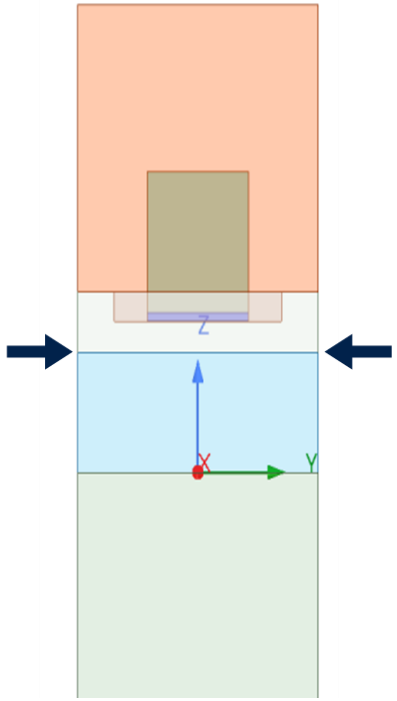
TCAD view

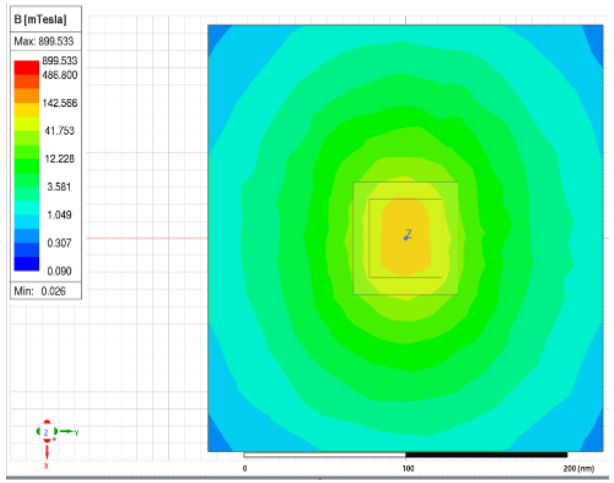
Simulation of a new transistor structure including magnetic material

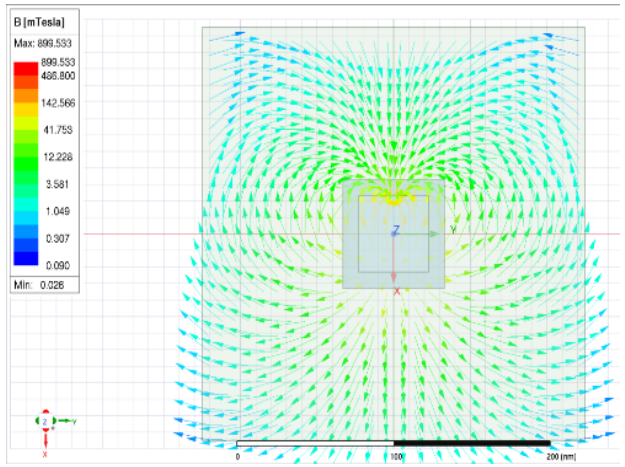
B. Doris, Solid-State Electronics, [2016]

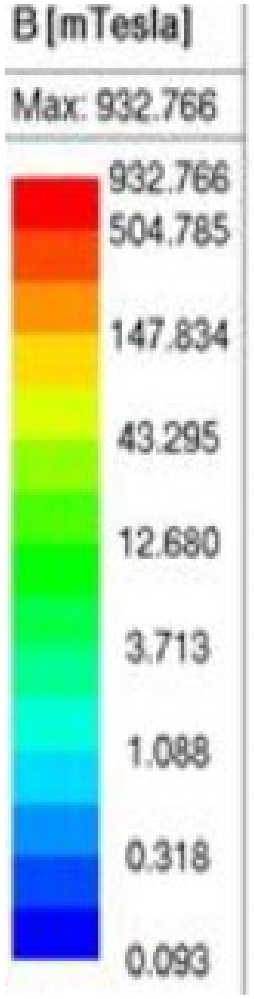
New device proposal – Transistor with magnetic gate

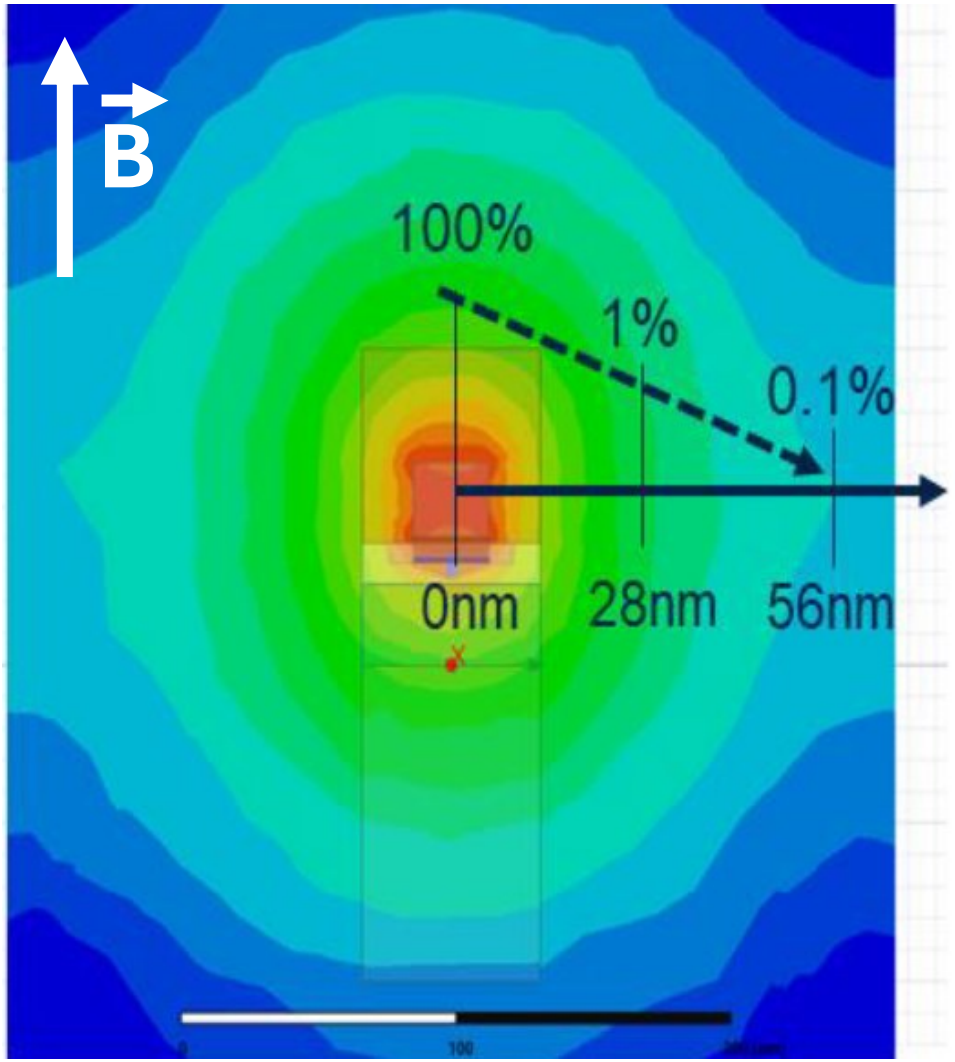
Plan z=25.5 nm











Sufficient magnetic field to drive qubit

Conclusion

- Multidisciplinary approach combining simulations, experimental characterization, materials and industrial integration
- Advances in the understanding of low-temperature magnetic materials
- Validation of cryogenic performance of integrated inductors for quantum applications
- New methods for improving the inductance of passive components in extreme environments

Perspectives

- Patterning of the magnetics material deposed around the ST inductors
- Integration of NbN in industrial CMOS BEOL
- Measure superconducting state of aluminum in CMOS inductor
- Integrate those inductor in a readout circuit and others design applications

Publications

- 1 Poster - Technology and design study of 3D physics based inductor on FDSOI for quantum and RF applications, **F. Sabatier,** C. Durand, D. Drouin, M. Pioro-Ladrière, E. Dupont-Ferrier, F. Ndagijimana, Ph. Galy, EUROSOI-ULIS 2023 (Tarragone)

- 1 Journal special issue and poster : Technology and design study of 3D physics-based inductor on FDSOI in GHz-range, **F. Sabatier**, C. Durand, D. Drouin, M. Pioro-Ladrière, F. Ndagijimana, Ph. Galy, *Solid-State Electronics,* 2023

- 1 Oral presentation : Preliminary numerical study on magnet gate in MOS FD-SOI technology for quantum and sensor applications; Ph. Galy, **F. Sabatier**, F. Ndagijimana, D. Drouin*, EUROSOI-ULIS,* 2024 (Athènes)

- 2 Patents:
  - Composant électronique comprenant une structure de grille, **F. Sabatier**, Ph. Galy, (internal ST reference: 22-GR1CO-1240FR01), 2023
  - CoSi2 solution for supra-conduction at cryogenic temperature compliant with CMOS bulk & FD-SOI substrate, M. Gregoire, **F. Sabatier**, Ph. Galy, (Internal ST reference : 24 GR1 0381), 2024

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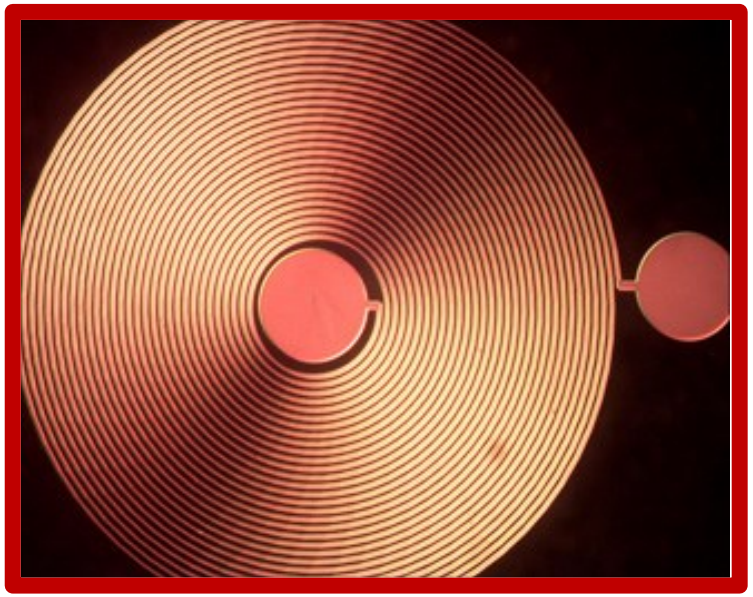
You have all greatly enriched my PhD experience and contributed to its success.

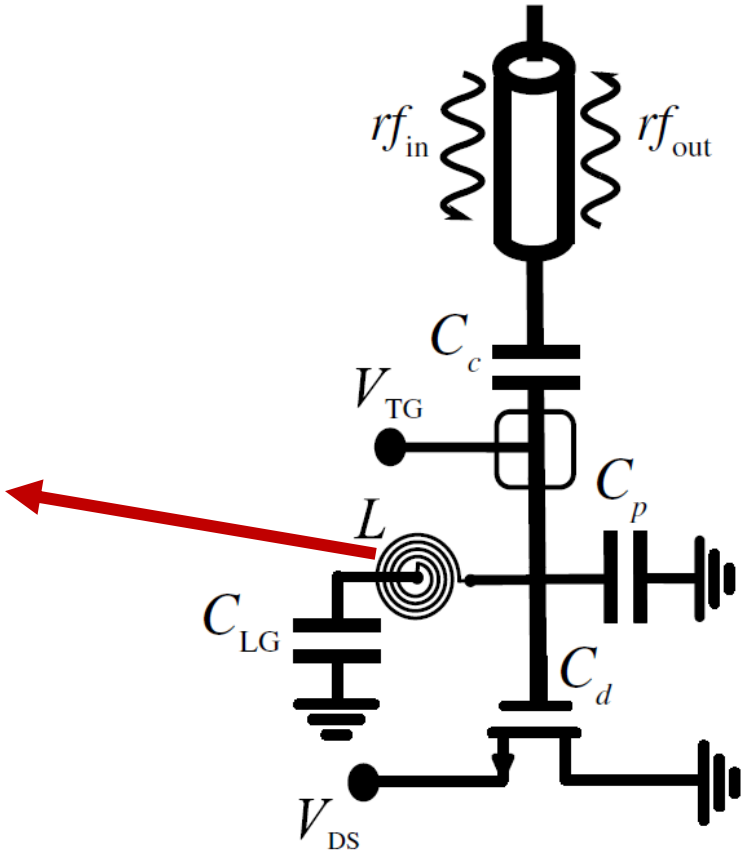
Questions session

Thank you for your kind attention.

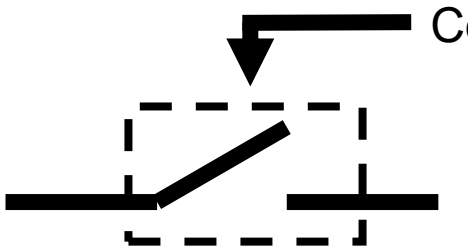
Back up slides

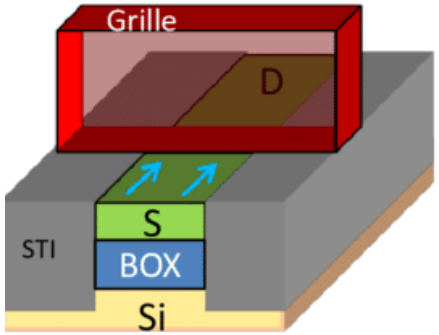
Selected paper of literature



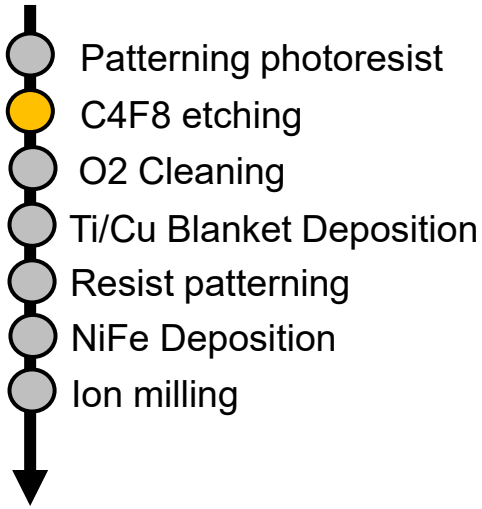


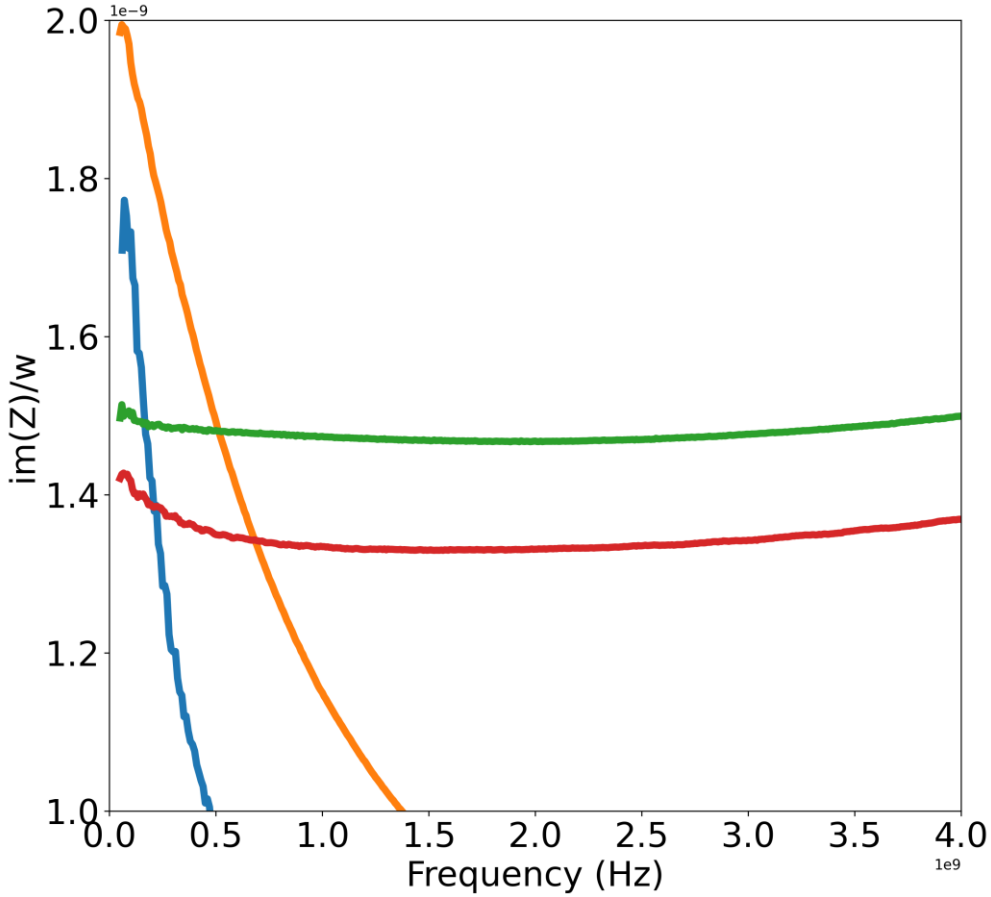
I. Ahmed and all, Phys. Rev. Appl., [2018]

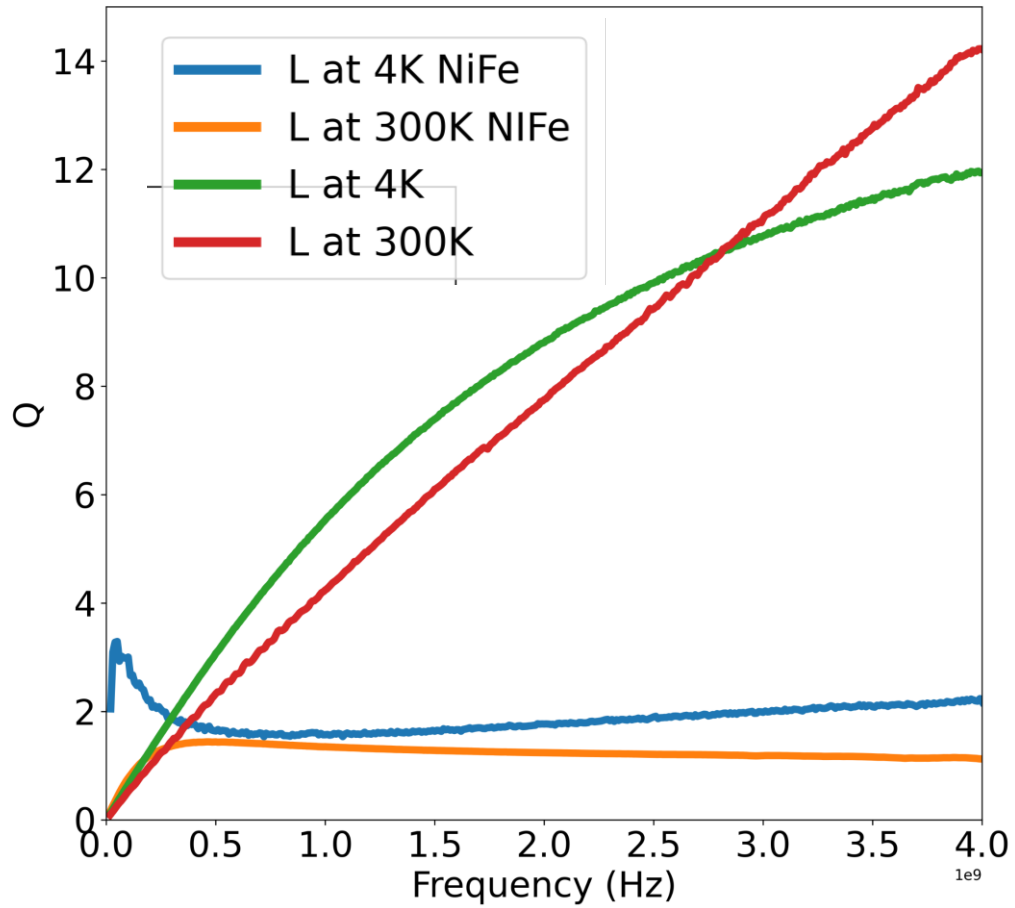

Control voltage


Grille
D
S
STI
BOX
Si

Process flow:




1e−9
2.0
1.8
1.6
1.4
1.2
1.0
im(Z)/w
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
1e9
Frequency (Hz)


L at 4K NiFe
L at 300K NIFe
L at 4K
L at 300K
14
12
10
8
6
4
2
0
Q
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
1e9
Frequency (Hz)